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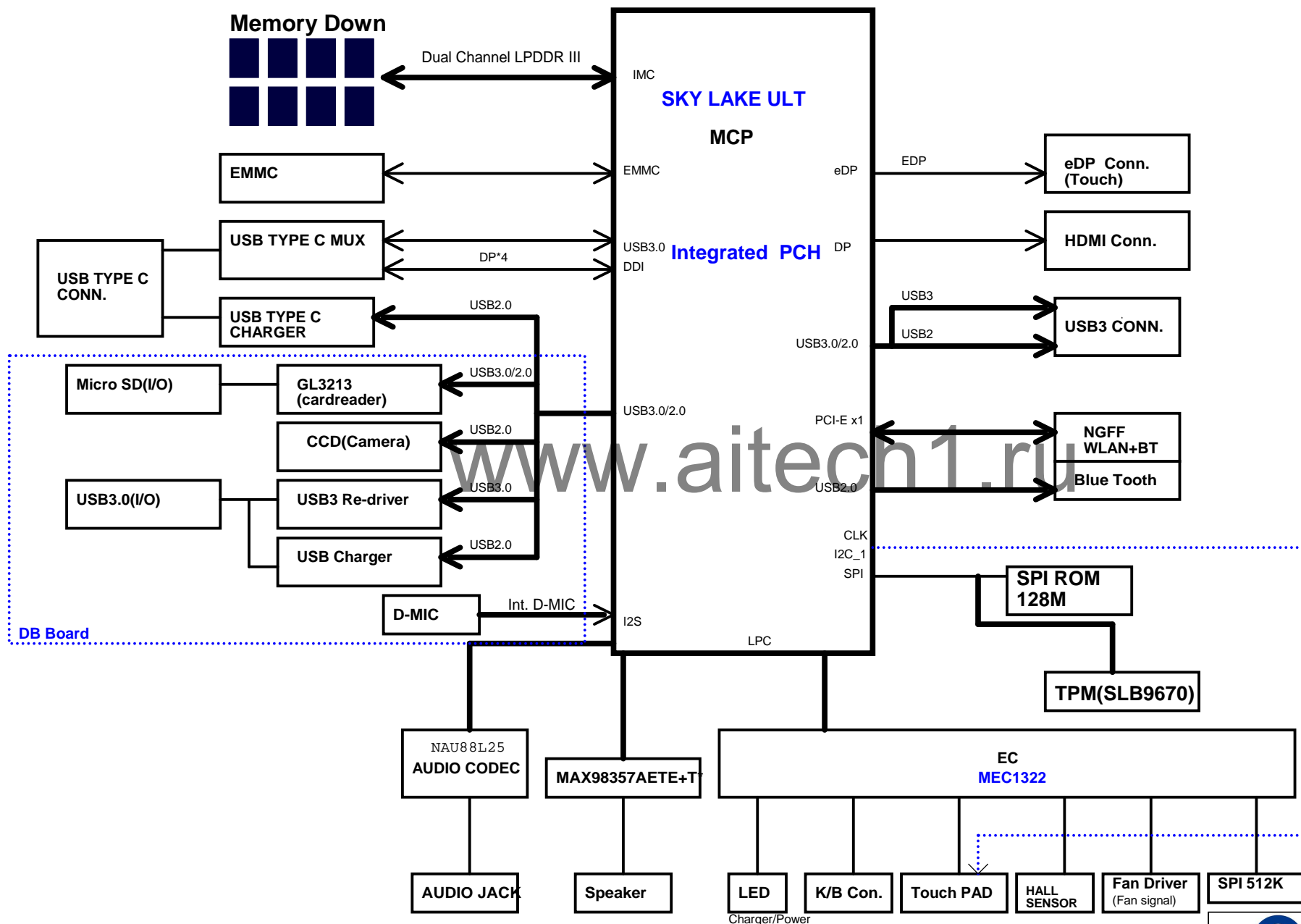
EU1B2 ,EUCP4040 ,U135 ,X5
 CN4 ,J1P2 ,CN3 ,LCP4022 ,LCP4041 ,J8L1 ,U8 ,SW1 ,J1C1 ,U97 ,U98
 ,CN12 ,CN8 ,U1 ,U23 ,UAP1012 ,CRCP4008 ,CRCP4009 ,CRCP4010
 ,CRCP4011 ,CRCP4014 ,CRCP4043 ,CRCP4042 ,CRCP4044 ,UCP4034
 ,UCP4036 ,UCP4040

Notes:

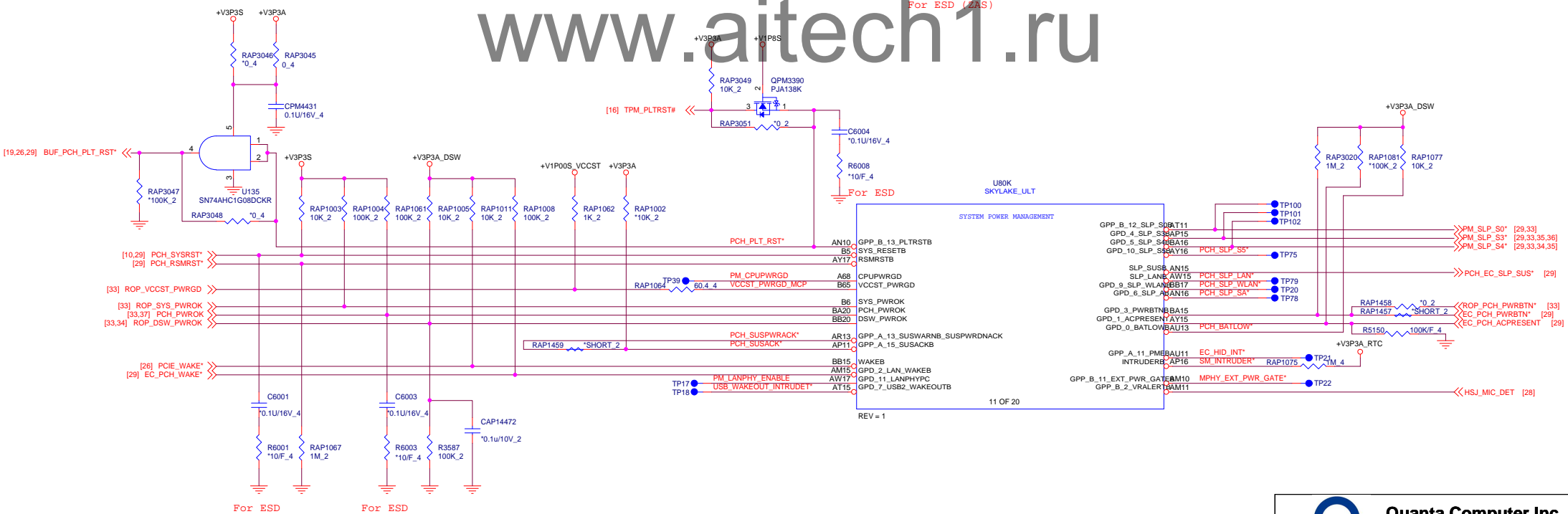
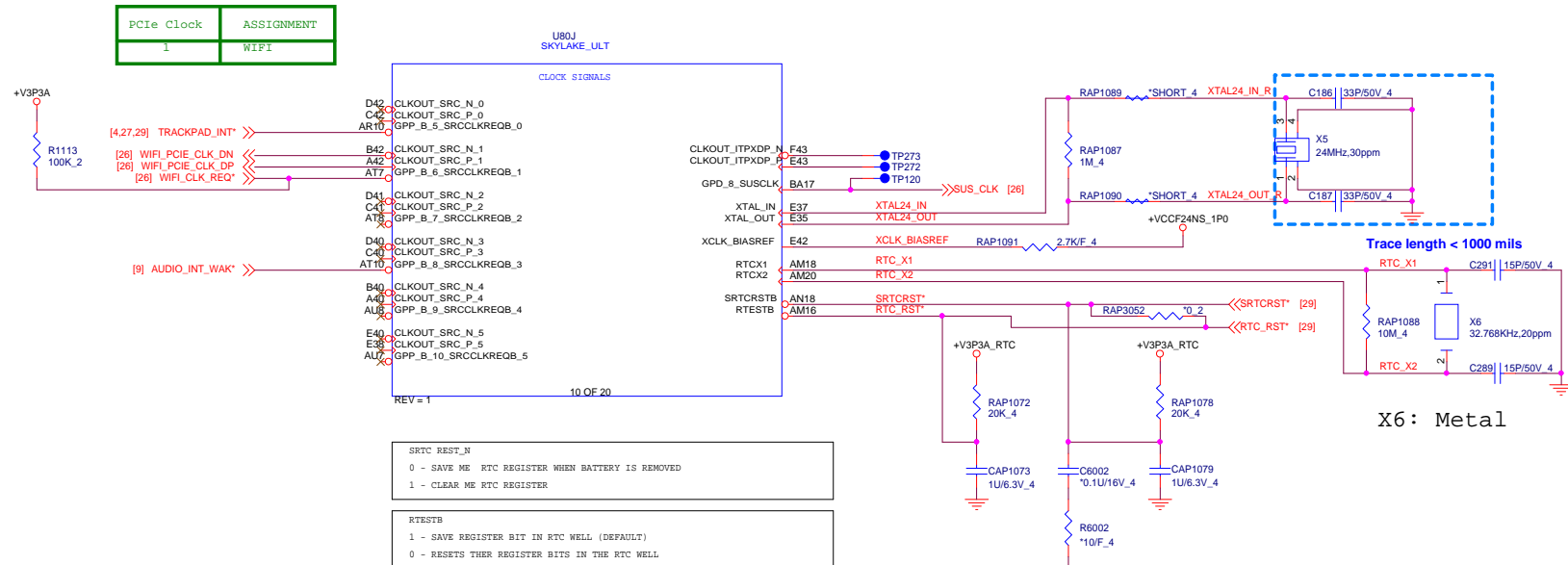
Part Value Prefix : "*" means no stuff
 Net Value suffix : "*" means Low Active
 Part : "*" means NO STUFF

ZHD SKL ULT SYSTEM BLOCK DIAGRAM

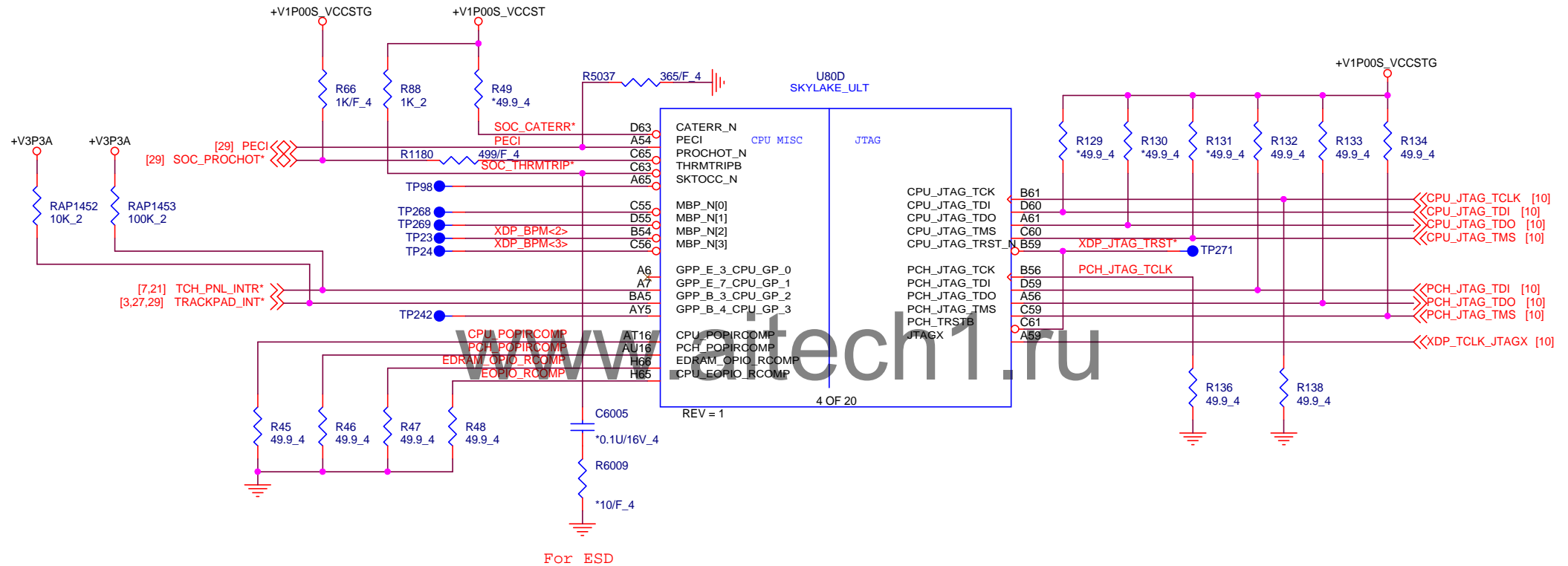
02



SKL ULT - SYSTEM CTL



SKL ULT - DEBUG

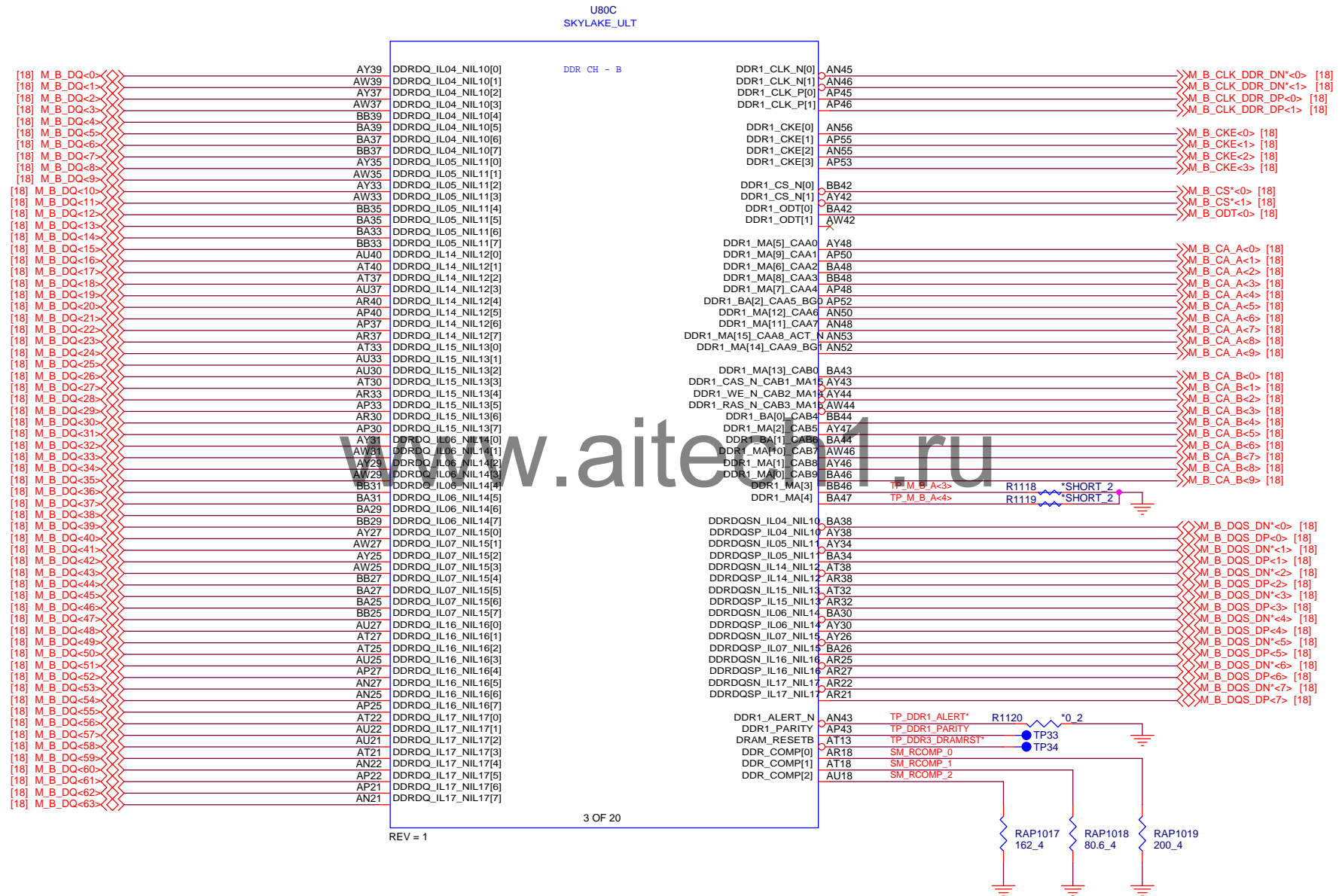


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Date: Tuesday, May 23, 2017	SKL ULT - DEBUG	
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SKL ULT - DDR CHANNEL B



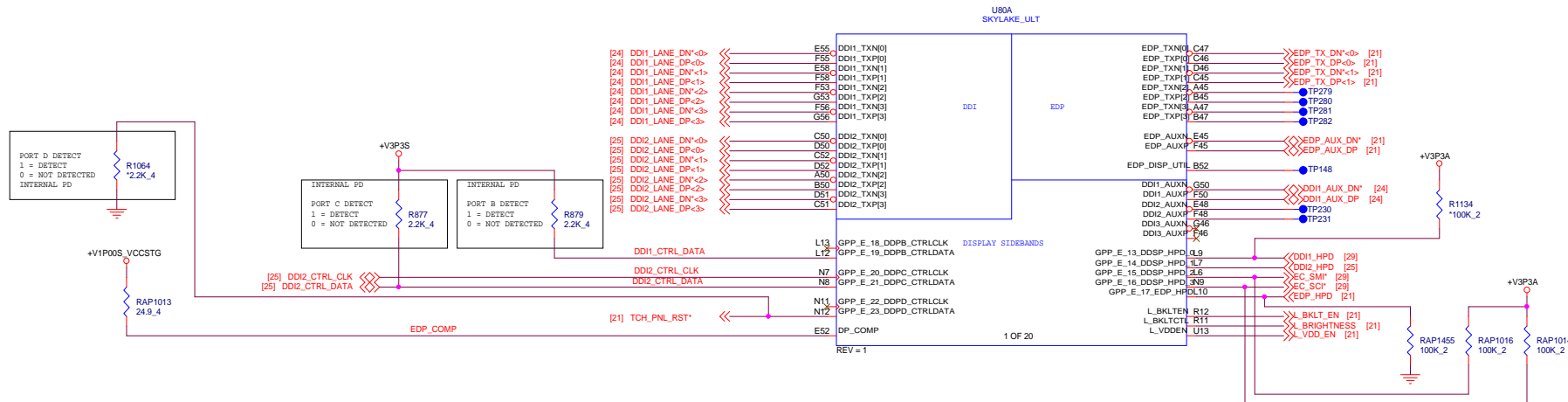
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SKL ULT - PCIE/SATA/USB/SSIC/DSI/CSI



USB3 PORT	USB2 PORT	ASSIGNMENT
1	1	USBC CONN
--	2	CCD
--	3	BLUETOOTH
4	9	USB-A CONN
3	5	USB 3.0 Conn.
2	6	Card reader

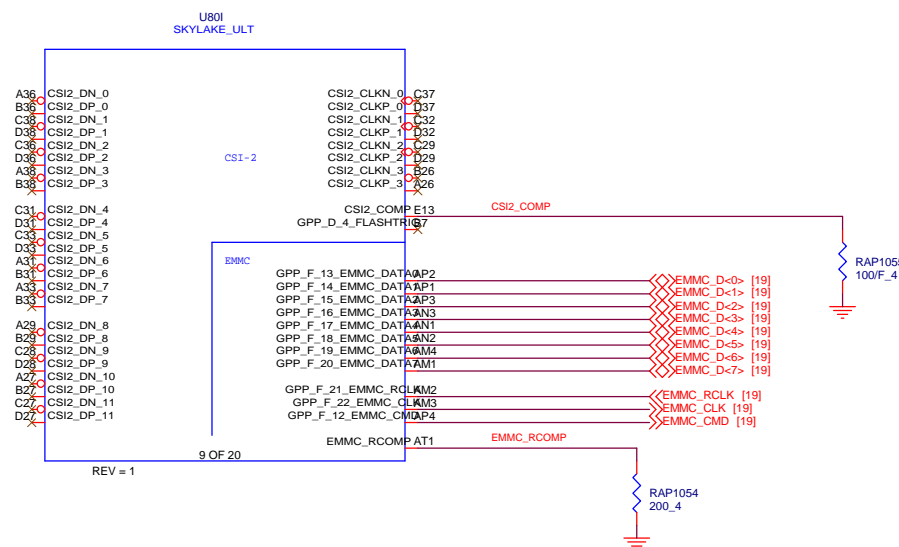
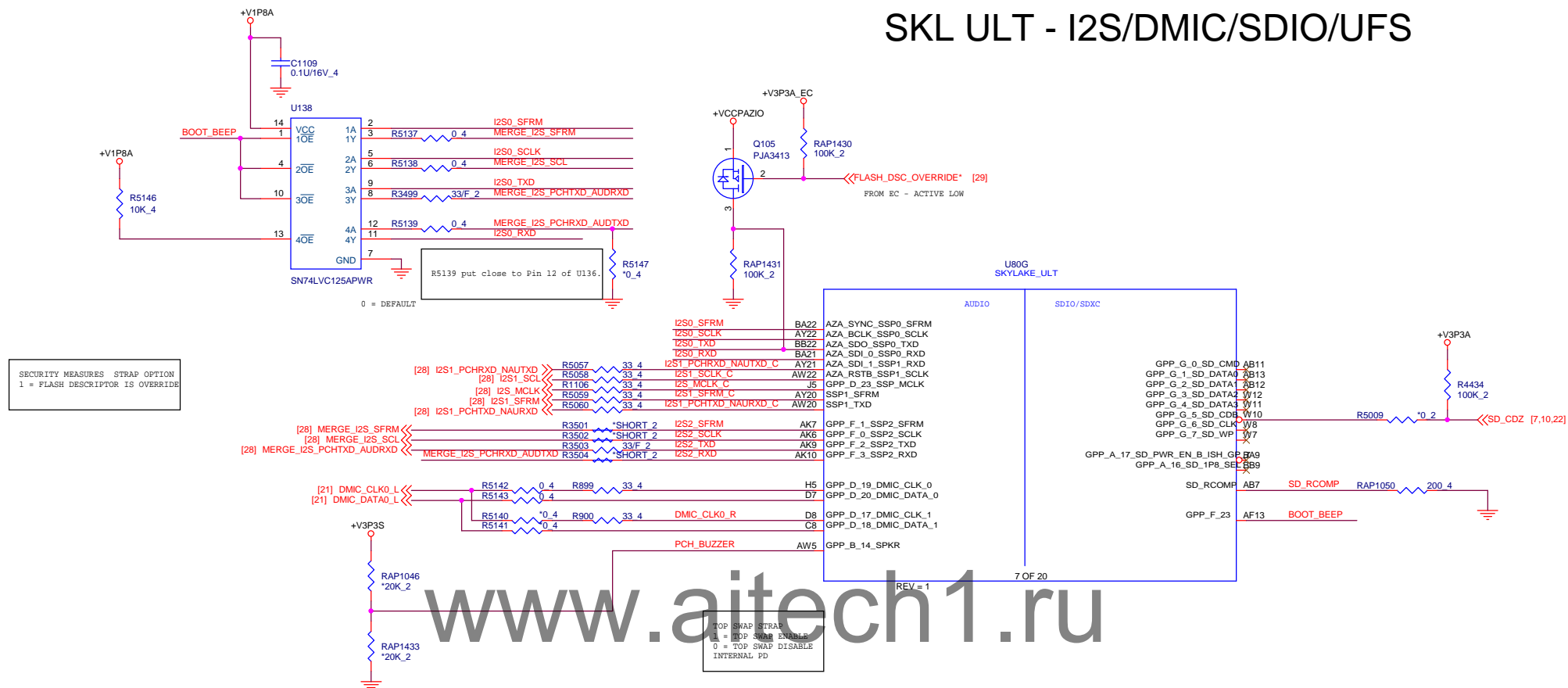
PCIE	SATA	ASSIGNMENT
1	--	WIFI

RING OSC BYPASS
1 = BYPASS MODE ENABLE
0 = RING OSC
QUALIFIED BY DPKTESTMODE

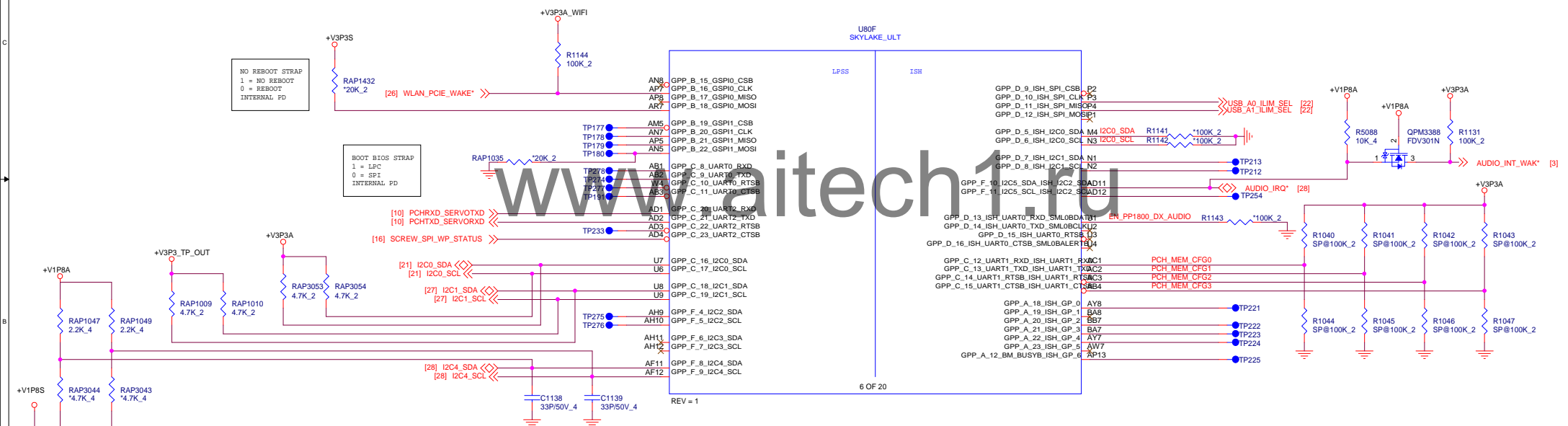
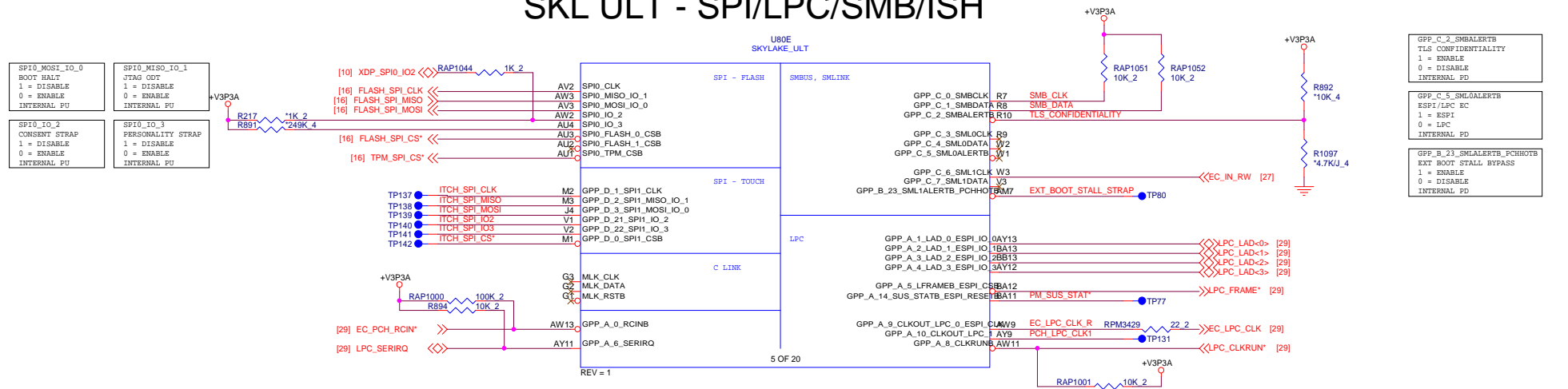
XTAL INPUT FREQ[1:0]
00 = 24 MHZ
01 = 25 MHZ
10 = 250 MHZ
11 = 100 MHZ
QUALIFIED BY DPKTESTMODE
HVM ONLY REMOVED IN SPT

XTAL INPUT FREQ[1:0]
00 = 24 MHZ
01 = 25 MHZ
10 = 250 MHZ
11 = 100 MHZ
QUALIFIED BY DPKTESTMODE
HVM ONLY REMOVED IN SPT

XTAL INPUT MODE (HVM ONLY)
1 = INPUT DIFFERENTIAL
0 = INPUT SINGLE-ENDED
QUALIFIED BY DPKTESTMODE



SKL ULT - SPI/LPC/SMB/ISH



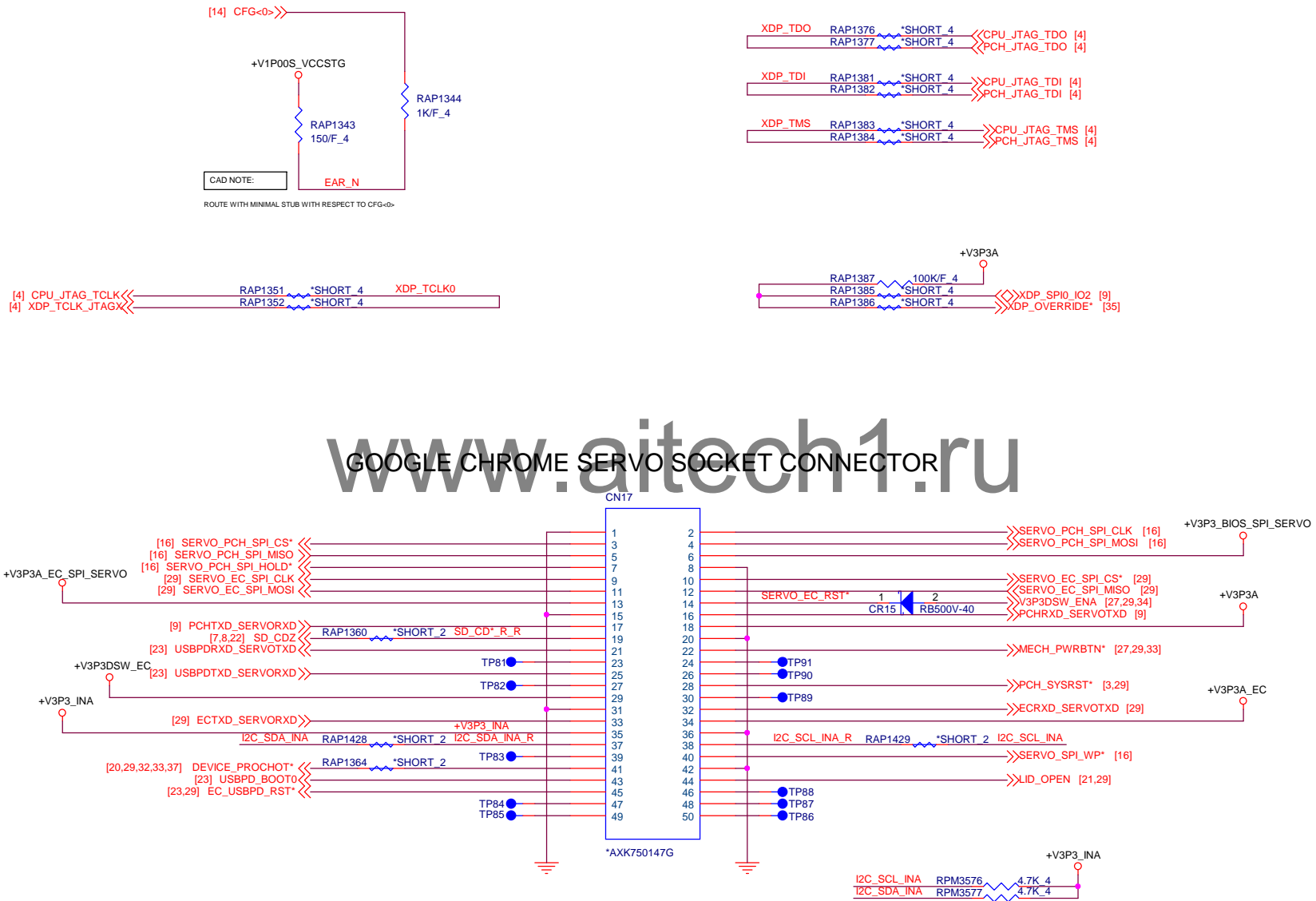
Memory straps pin

I2C PORT	ASSIGNMENT	LEVEL
0	RESERVED	+3.3V
1	TRACKPAD	+3.3V
2	NFC	+1.8V
3	RESERVED	+1.8V
4	AUDIO CODEC	+1.8V
ISH 0	ISH	+1.8V

PCH_MEM_CFG[3:0]	MEMORY PN	Specification	Stuff
0 0000	H9CCNNN8JTBLAR-NUD	(HYX ,SINGLE CHANNEL (2PCS) , 2GB, 1866Mbps)	R1044,R1045,R1046,R1047
1 0001	H9CCNNNBLTBLAR-NUD	(HYX , DUAL CHANNEL (4PCS) , 8GB, 1866Mbps)	R1040,R1045,R1046,R1047
2 0010	K4E88324EB-EGCF	(SAM , DUAL CHANNEL (4PCS) , 4GB, 1866Mbps)	R1044,R1041,R1046,R1047
3 0011	K4E88324EB-EGCF	(SAM ,SINGLE CHANNEL (2PCS) , 2GB, 1866Mbps)	R1040,R1041,R1046,R1047
4 0100	H9CCNNNBLTBLAR-NUD	(HYX ,SINGLE CHANNEL (2PCS) , 4GB, 1866Mbps)	R1044,R1045,R1042,R1047
5 0101	K4E66304EB-EGCF	(SAM , DUAL CHANNEL (4PCS) , 8GB, 1866Mbps)	R1040,R1045,R1042,R1047
6 0110	H9CCNNN8JTBLAR-NUD	(HYX , DUAL CHANNEL (4PCS) , 4GB, 1866Mbps)	R1044,R1041,R1042,R1047
7 0111	H9CCNNNBJTBLAR-NUD	(HYX ,SINGLE CHANNEL (2PCS) , 4GB, 1866Mbps)	R1040,R1041,R1042,R1047
8 1000	MT52L256M32D1PF-107	(MIC , DUAL CHANNEL (4PCS) , 4GB, 1866Mbps)	R1044,R1045,R1046,R1047
9 1001	MT52L512M32D2PF-107	(MIC , DUAL CHANNEL (4PCS) , 8GB, 1866Mbps)	R1040,R1045,R1046,R1047
10 1010	H9CCNNN8GTALAR-NUD	(HYX , DUAL CHANNEL (4PCS) , 4GB, 1866Mbps)	R1044,R1041,R1046,R1047
11 1011	MT52L512M32D2PF-107	(MIC , SINGLE CHANNEL (2PCS) , 4GB, 1866Mbps)	R1040,R1041,R1046,R1047

K4E6E304EB-EGCF (2GB, 1866Mbps)
EDF8132A3MA-JD-F (1GB, 1866Mbps)

SKL ULT - XDP/CHROME SERVO



U80L
SKYLAKE_ULT

CPU POWER 1 OF 4

+VCCCORE

+VCCCORE

A30 VCCCORE

A34 VCCCORE

A39 VCCCORE

A44 VCCCORE

AK33 VCCCORE

AK35 VCCCORE

AK37 VCCCORE

AK38 VCCCORE

AK40 VCCCORE

AL33 VCCCORE

AL37 VCCCORE

AL40 VCCCORE

AM32 VCCCORE

AM33 VCCCORE

AM35 VCCCORE

AM37 VCCCORE

AM38 VCCCORE

G30 VCCCORE

G32 VCCCORE

G33 VCCCORE

G35 VCCCORE

G37 VCCCORE

G38 VCCCORE

G40 VCCCORE

G42 VCCCORE

J30 VCCCORE

J33 VCCCORE

J37 VCCCORE

J40 VCCCORE

K33 VCCCORE

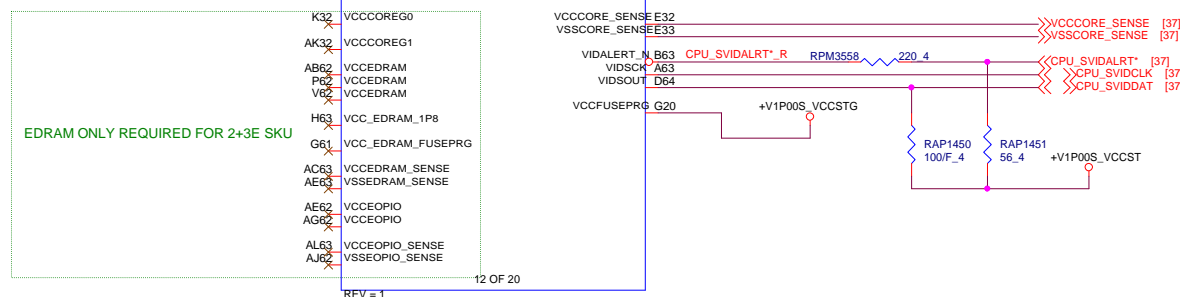
K35 VCCCORE

K37 VCCCORE

K38 VCCCORE

K42 VCCCORE

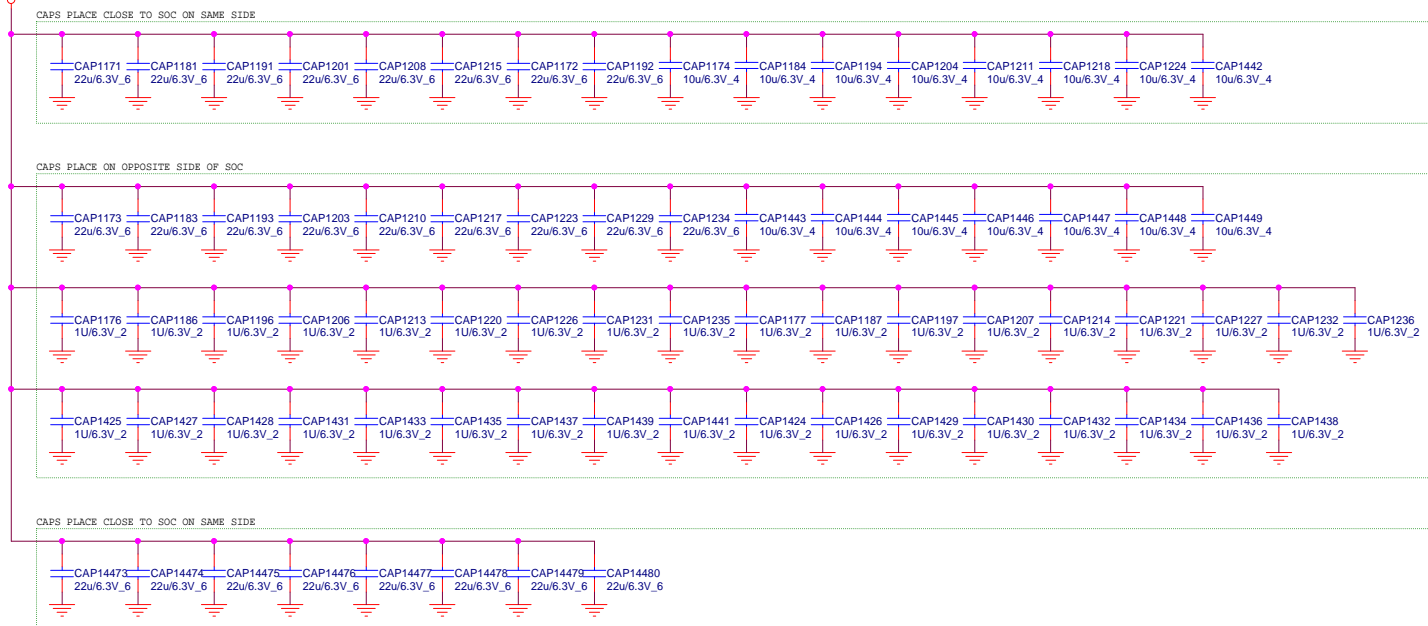
K43 VCCCORE



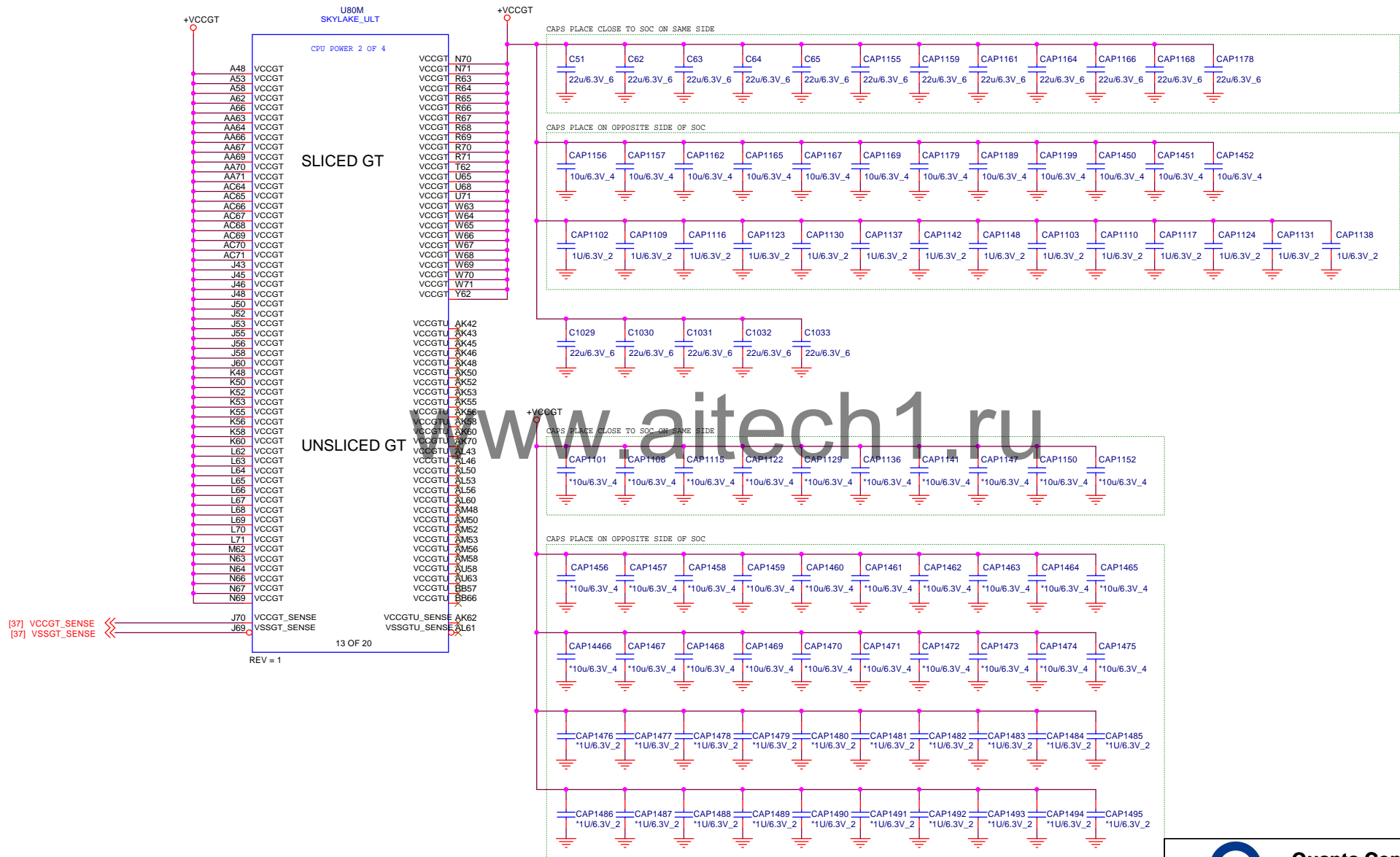
REV = 1

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+VCCCORE



SKL ULT - POWER GRAPHICS



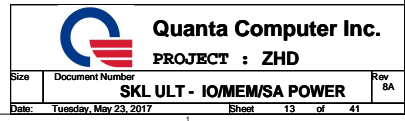
Quanta Computer Inc.

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Size	Document Number	Rev
	SKL ULT - GT POWER	8A

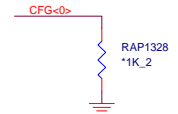
Date: Tuesday, May 23, 2017 Sheet 12 of 41

The schematic shows several power supply rails: +VCCPRM_CORE, +VCCPRM_1P0, +VCCPGPPA, +VCCPGPPB, and +VCCPGPPC. It includes two LM7805 voltage regulators, one for +VCCPRM_1P0 and another for +VCCPGPPA. There are also two 7805 regulators labeled B800 and SW900. Various capacitors are connected to these rails, including CAP1276, CAP1443, CAP1444, CAP1445, CAP1446, CAP1447, CAP1448, CAP1449, CAP1450, CAP1451, CAP1452, CAP1453, CAP1454, CAP1455, CAP1456, CAP1457, CAP1458, CAP1459, CAP1460, CAP1461, CAP1462, CAP1463, CAP1464, CAP1465, CAP1466, CAP1467, CAP1468, CAP1469, CAP1470, CAP1471, CAP1472, CAP1473, CAP1474, CAP1475, CAP1476, CAP1477, CAP1478, CAP1479, CAP1480, CAP1481, CAP1482, CAP1483, CAP1484, CAP1485, CAP1486, CAP1487, CAP1488, CAP1489, CAP1490, CAP1491, CAP1492, CAP1493, CAP1494, CAP1495, CAP1496, CAP1497, CAP1498, CAP1499, CAP1500.

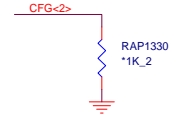


SKL ULT - RESERVED

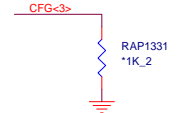
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1: (DEFAULT) NORMAL OPERATION; NO STALL 0: STALL



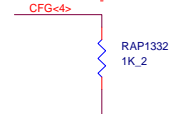
JUST A PLACEHOLDER - NO PEG FOR ULX/ULT	
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT) NORMAL OPERATION; 0: LANE REVERSAL



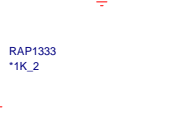
PHYSICAL DEBUG ENABLED (DFX PRIVACY)	
CFG3	0: ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1: DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

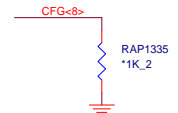


JUST A PLACEHOLDER. NOT NEEDED FOR ULX/ULT	
CFG5	

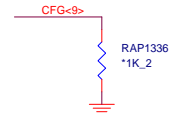


PCI PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION1, DEVICE 1 FUNCTION2 DISABLED 10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED 00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

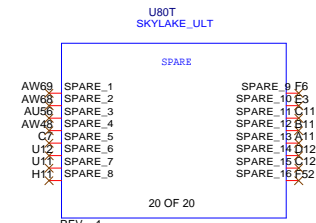
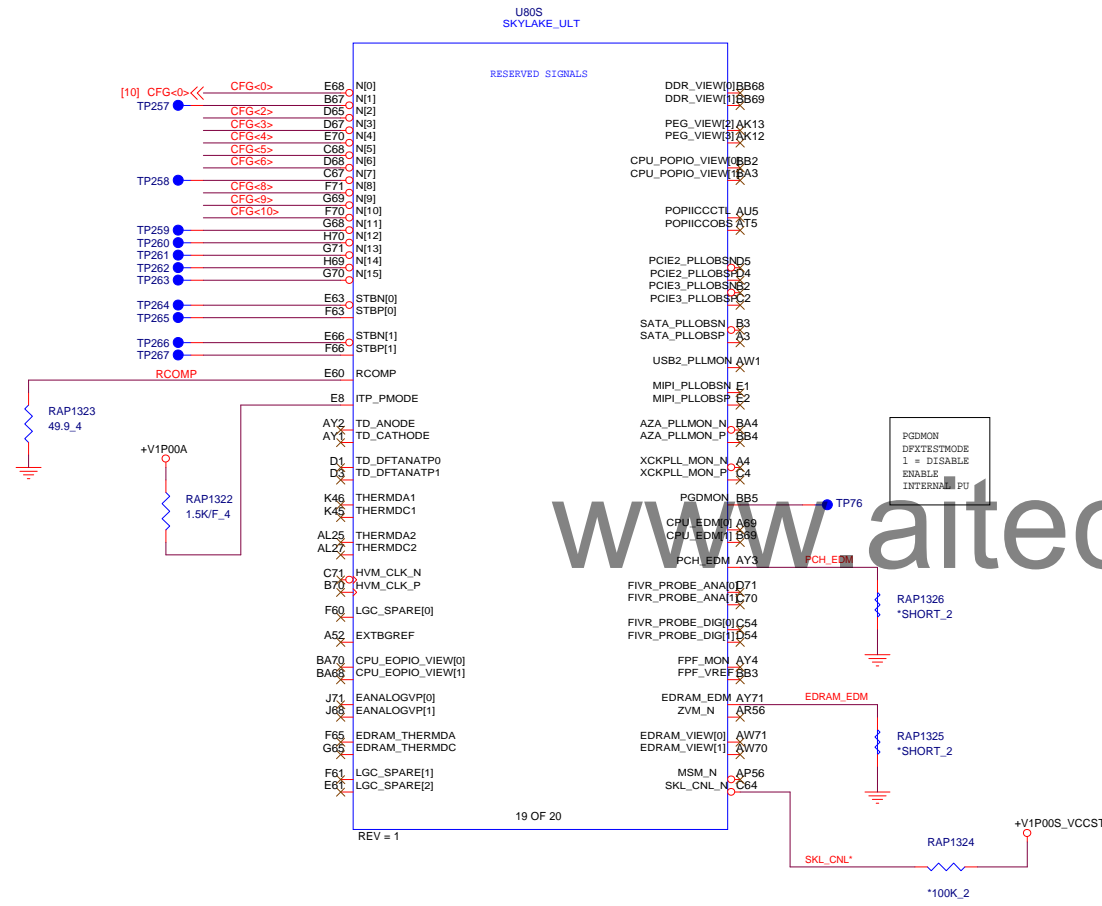
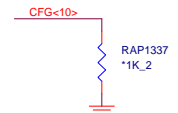
Reserve	
CFG8	1: DISABLED (DEFAULT) 0: ENABLED; WILL BE



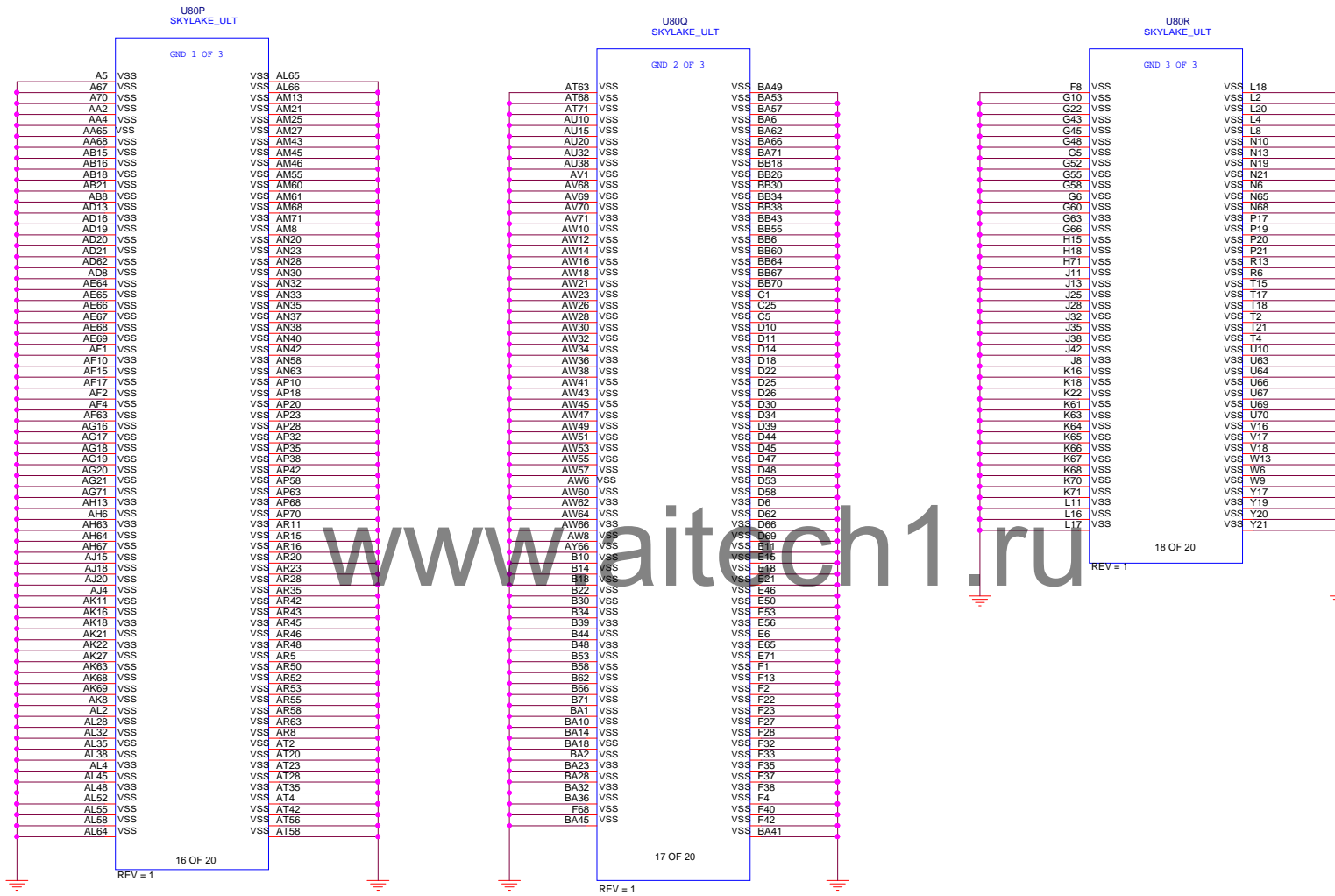
NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VR SUPPORTING SVID PROTOCOL ARE PRESENT 0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY



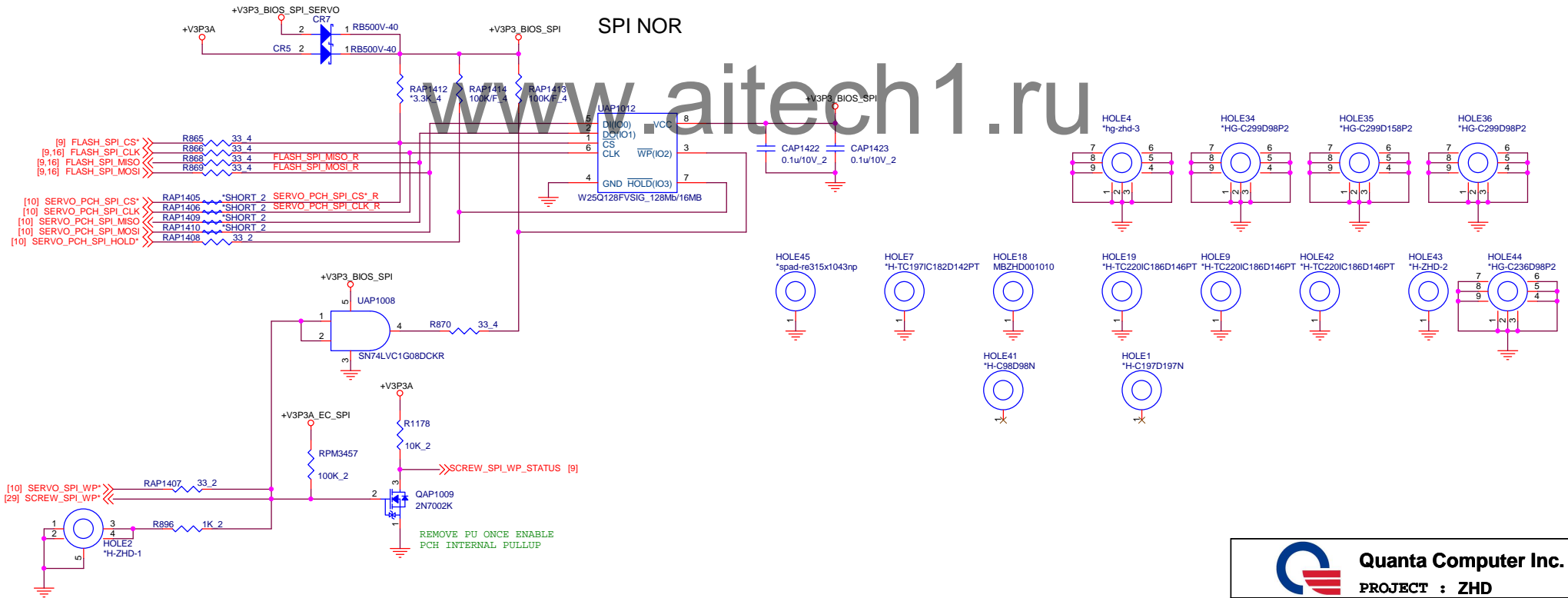
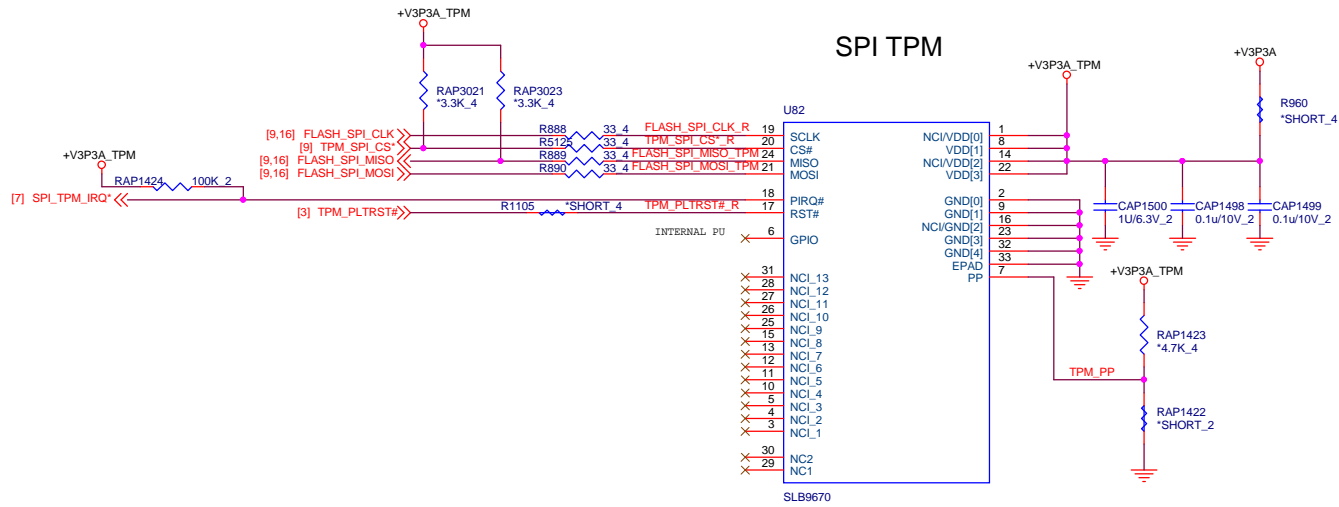
SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATING) ARE NOT ACTIVATED



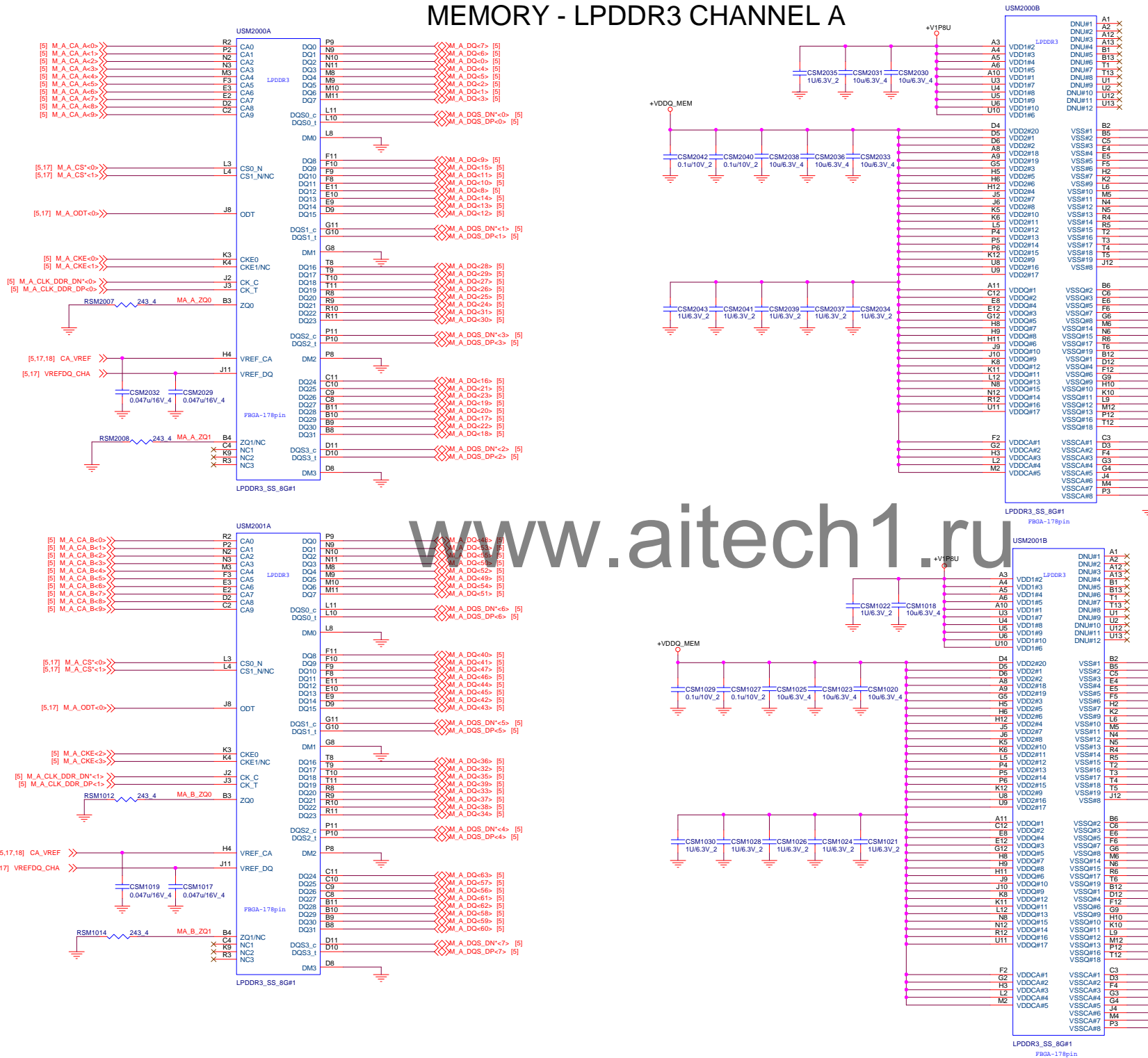
SKL ULT - GND



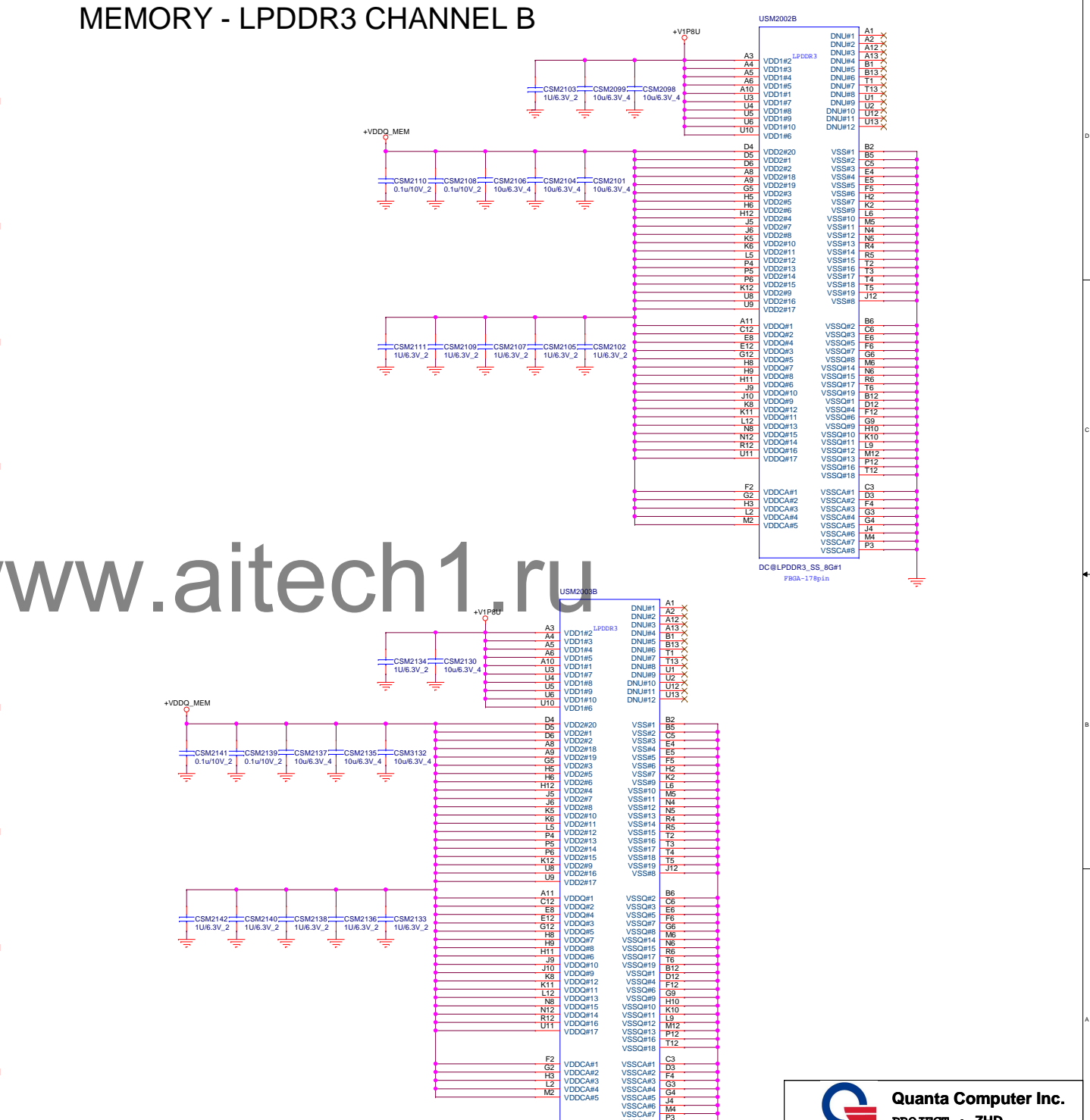
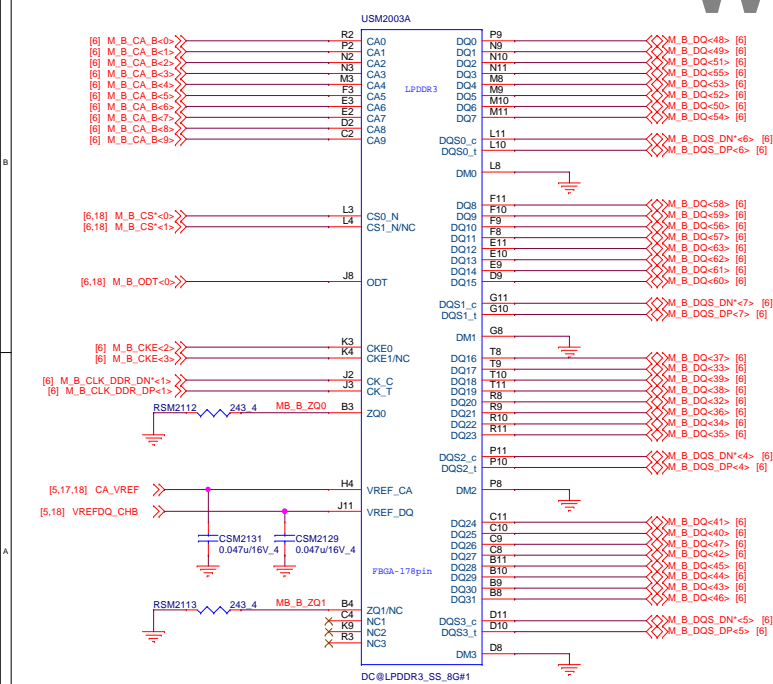
TPM & BOOT ROM



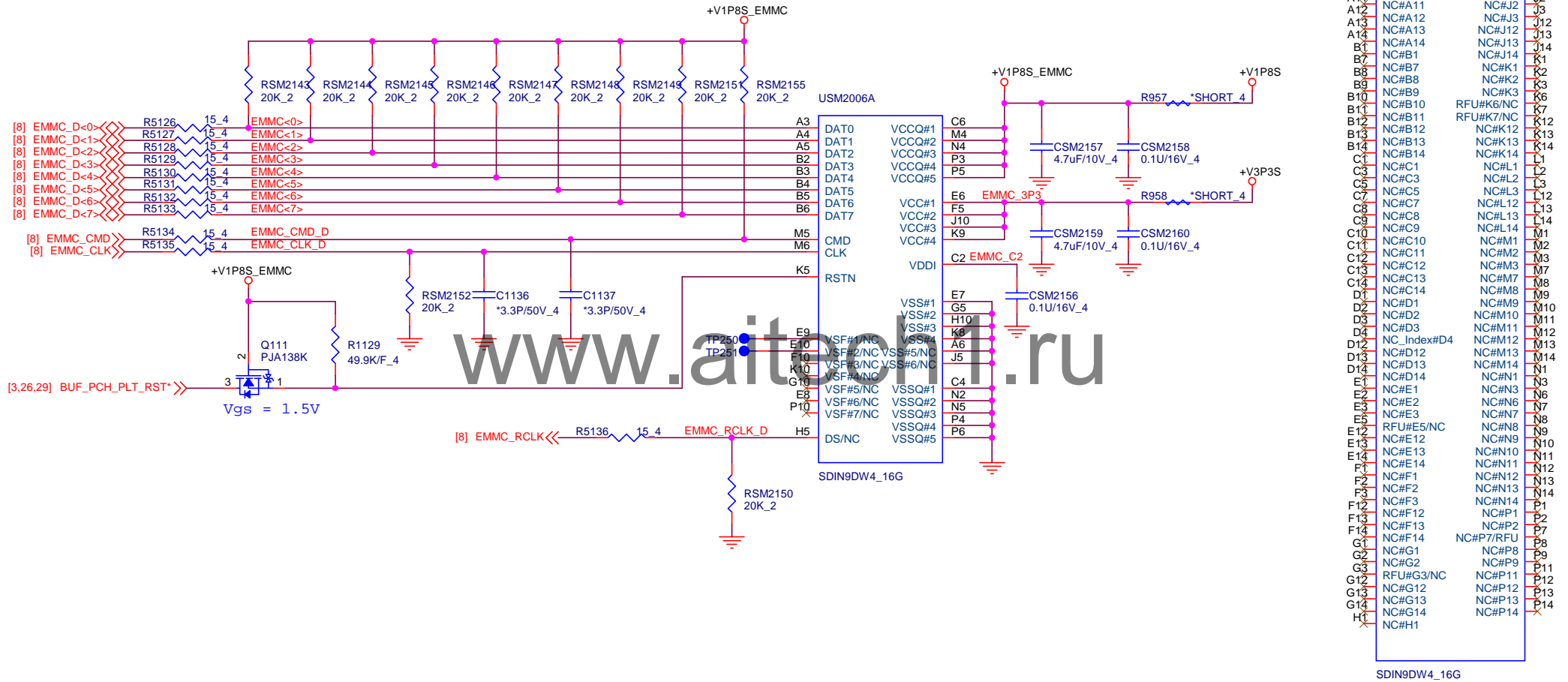
MEMORY - LPDDR3 CHANNEL A



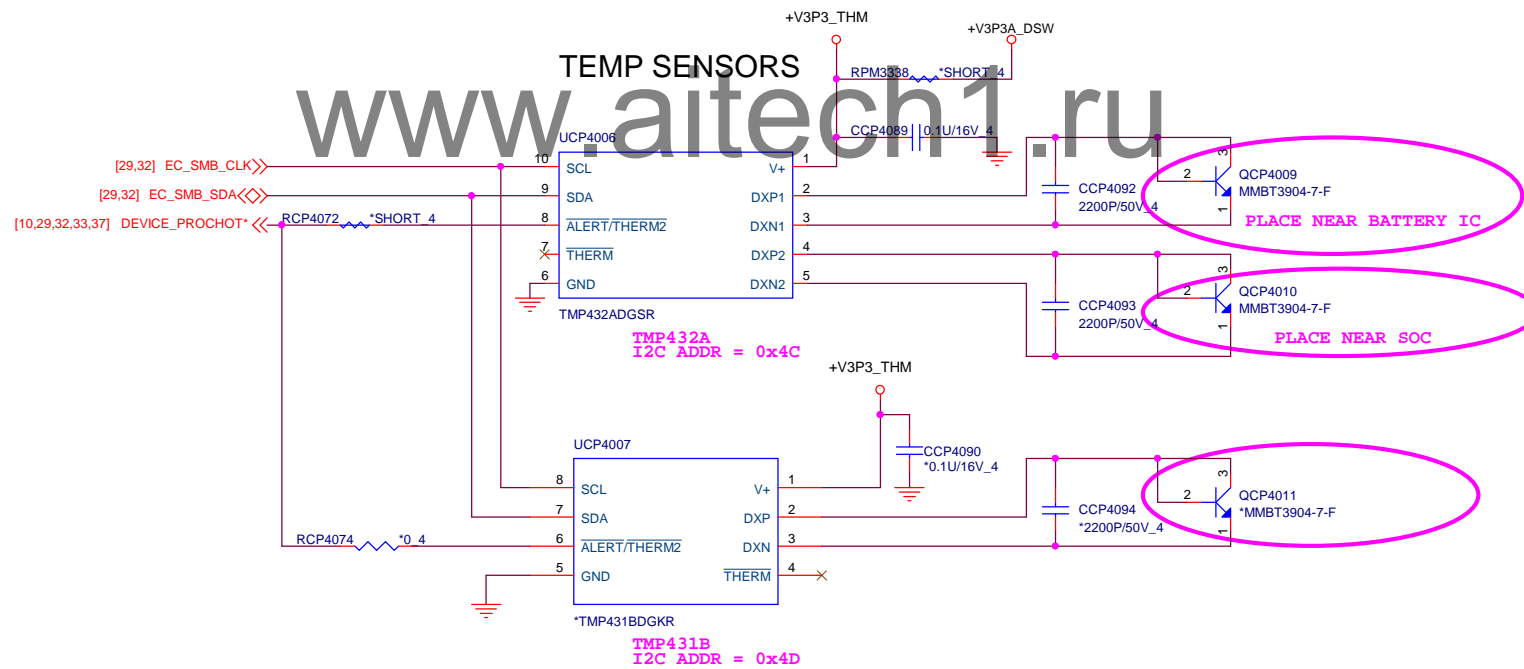
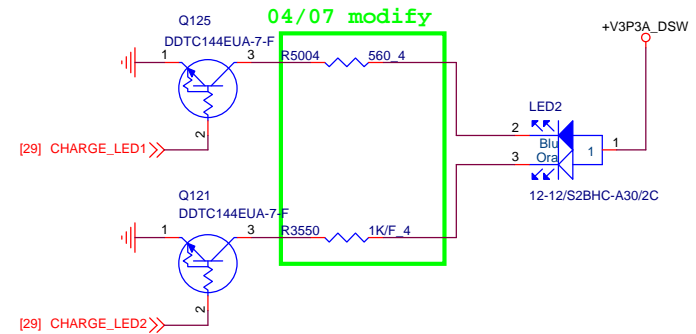
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EMMC



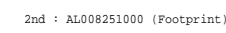
CHARGE LED STATUS



eDP DISPLAY PANEL

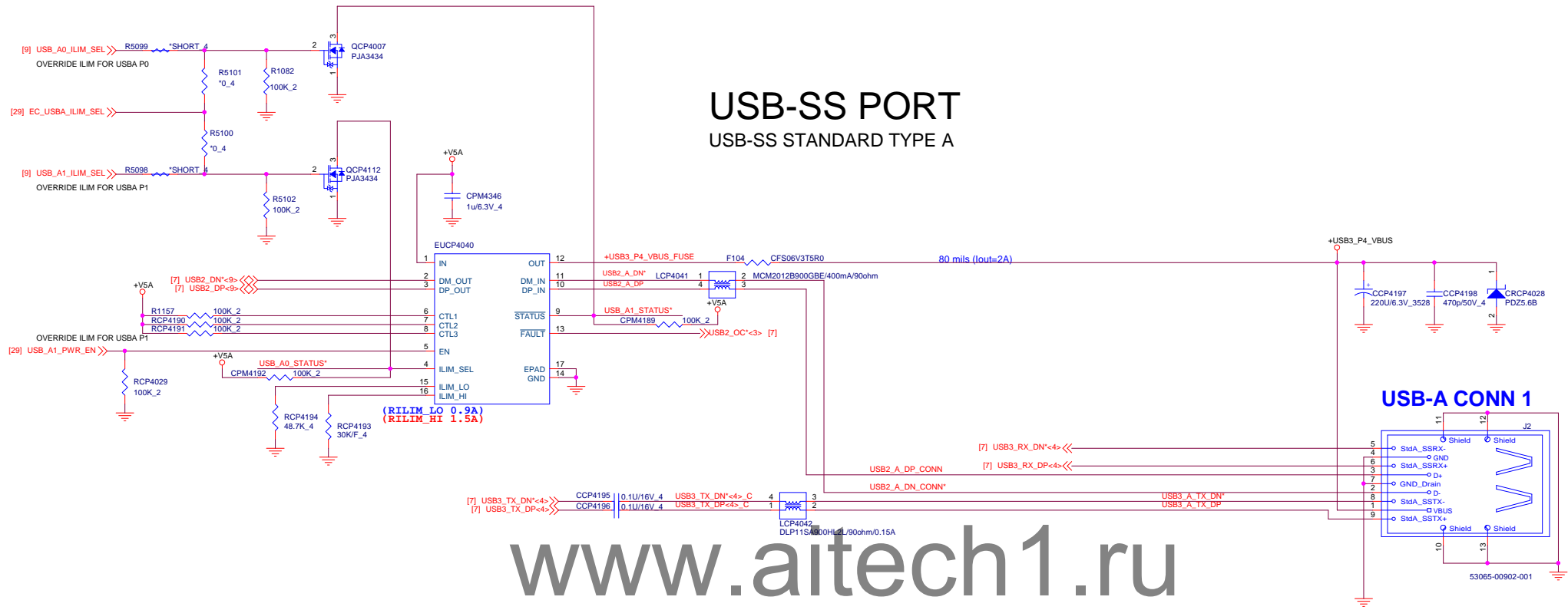


ZAV

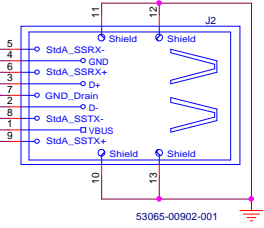


USB-SS PORT

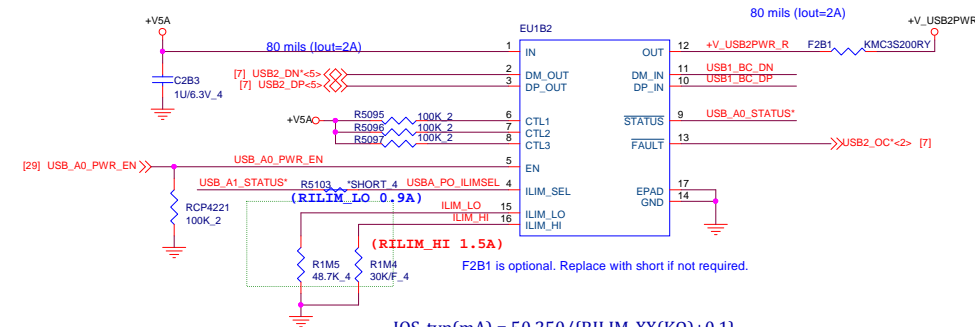
USB-SS STANDARD TYPE A



USB-A CONN 1

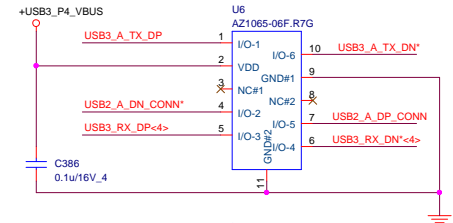


USB Charger



$$IOS_typ(mA) = 50,250 / (RILIM_XX(K\Omega) + 0.1)$$

Condition	CTL1	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
SDP2	1	1	1	0



USB protection diodes for ESD,
as close as possible to USB connector pins.

USB 3.0 (5V) 6CH
BC106506000 Amazing
BCD5326DZ00 willsemi
BC12010LZ00 INPAQ

Card Reader

USBC EC
CC NEGOTIATION

Table 2. FUNCTION TABLE

EN	IN	NO TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
H	H	OFF	ON
X	X	OFF	OFF

EN	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
H	H	OFF	ON
X	X	OFF	OFF

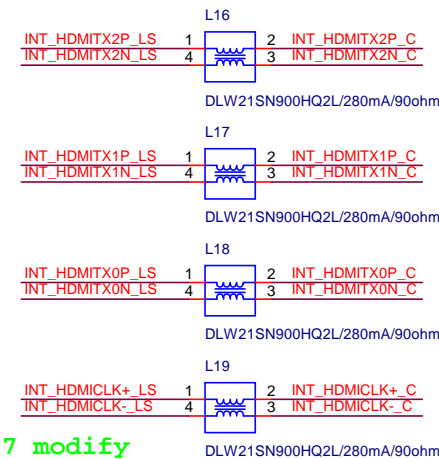
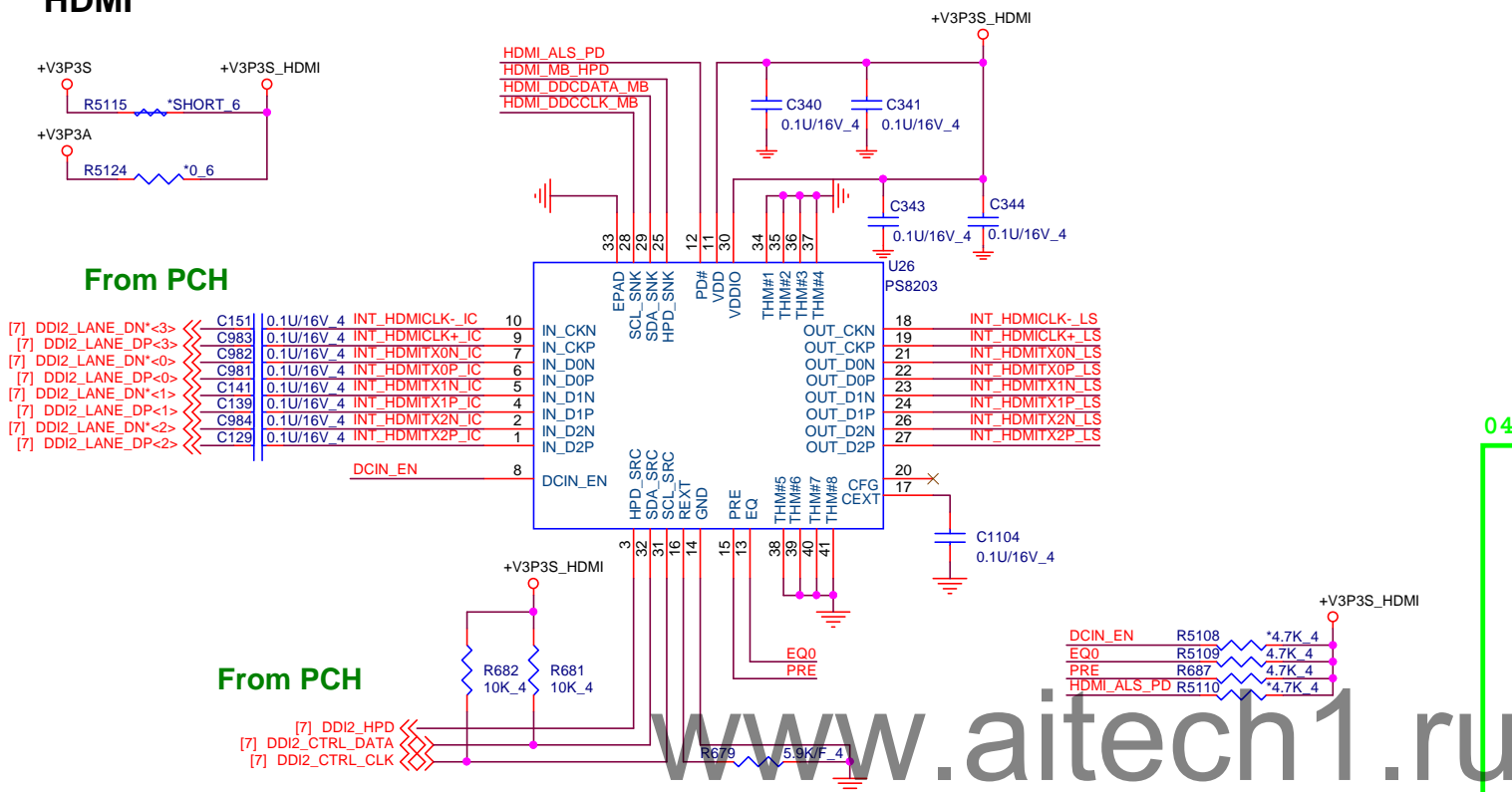
+V3P3A_DSW +V3P3DSW_DOR

R3620 *SHORT_4

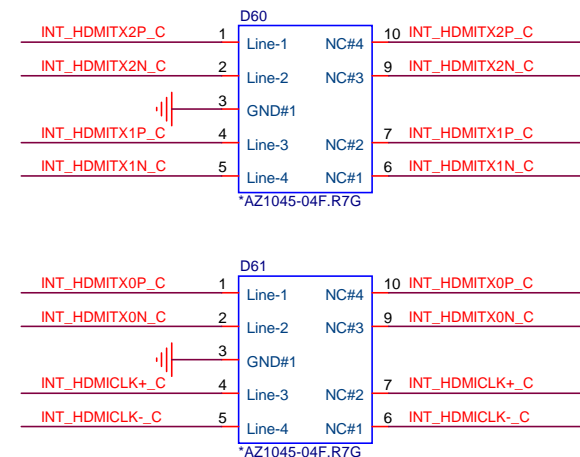
Rev
8A

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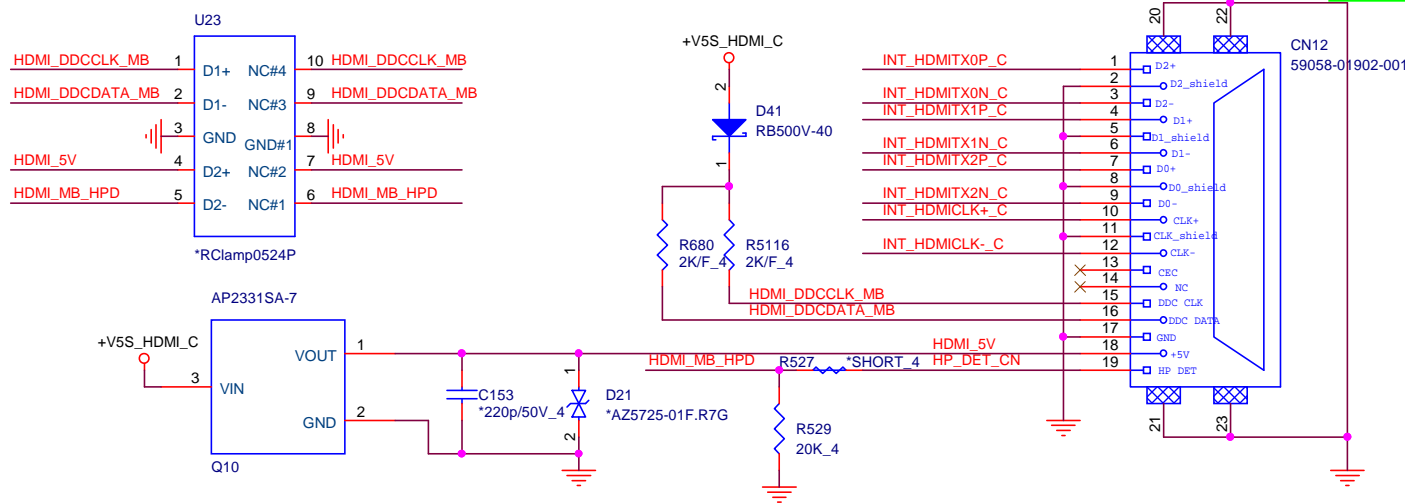
HDMI



04/07 modify



HDMI connector



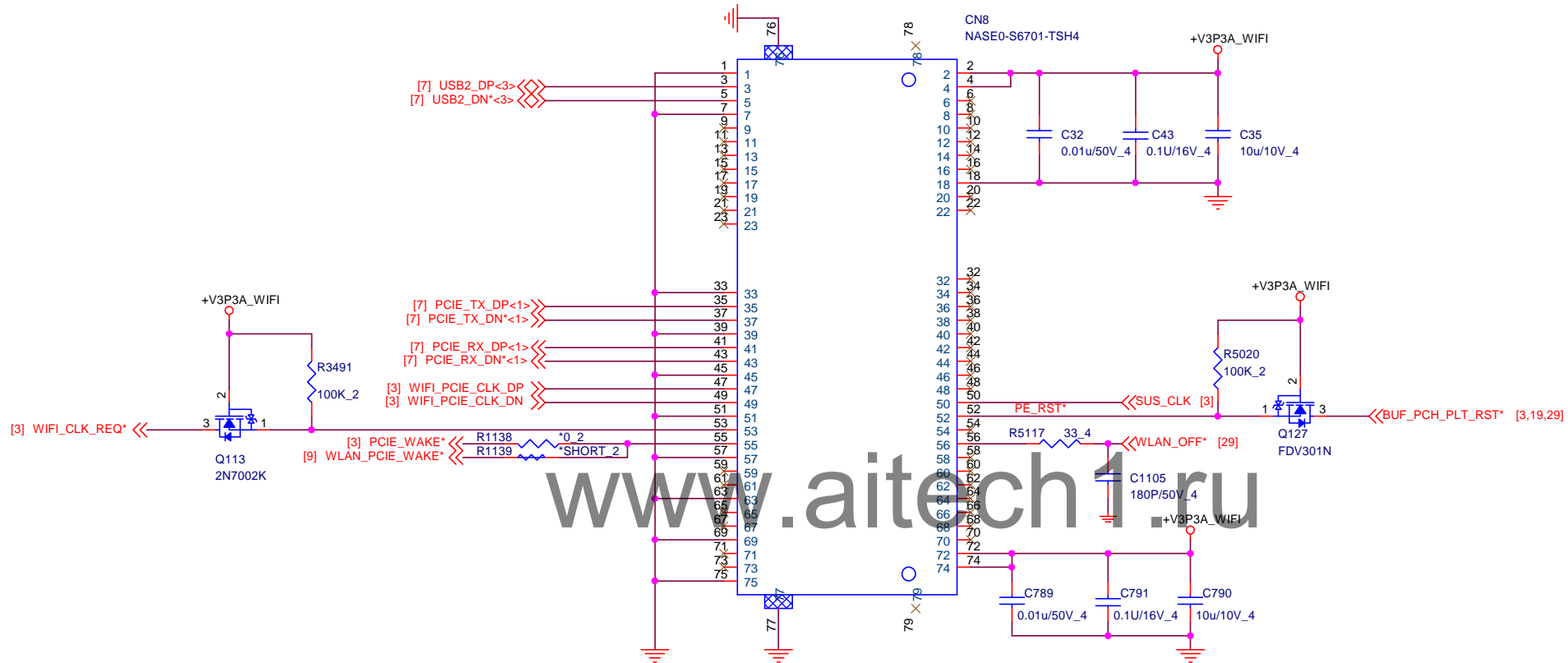
Quanta Computer Inc.

PROJECT : ZHD

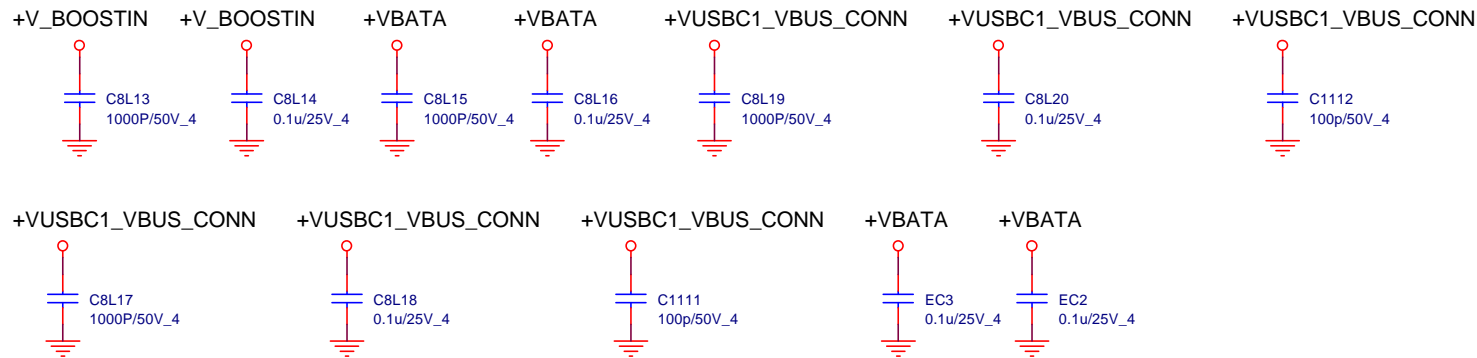
Size	Document Number	Rev
	HDMI	8A

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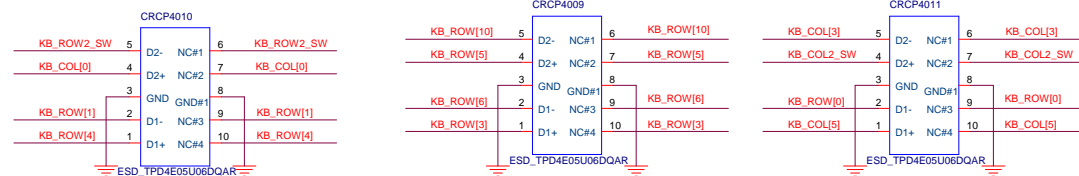
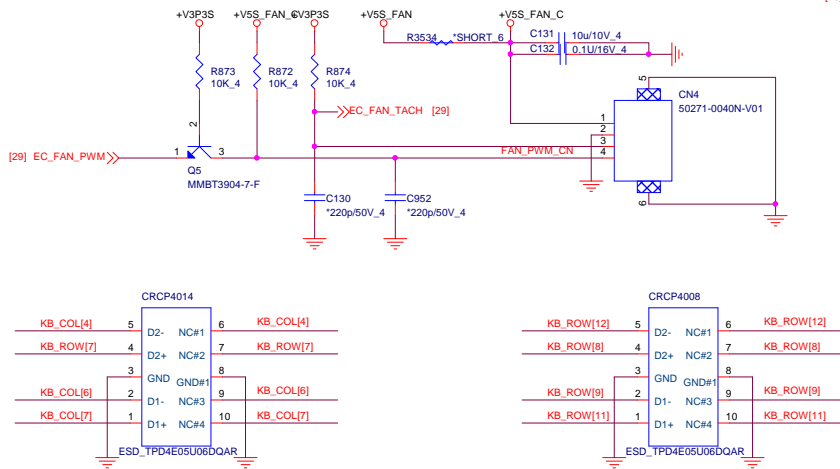
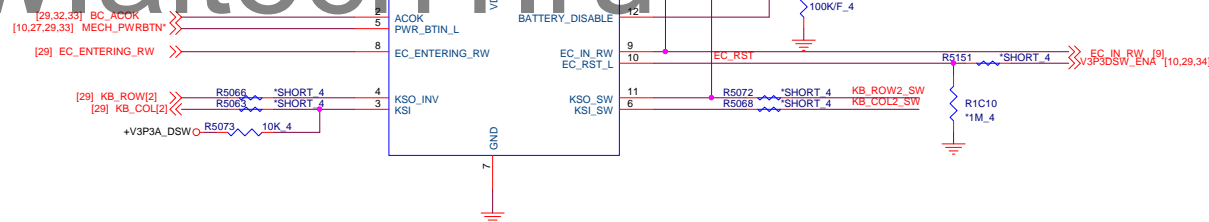
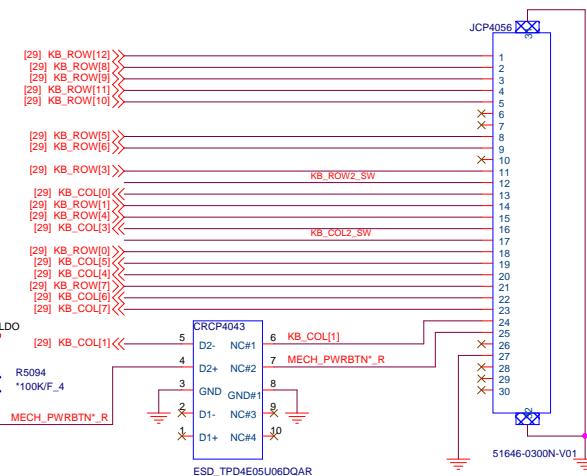
M.2 WIFI/BT NGFF WIFI



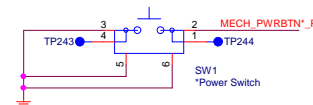
For EMI



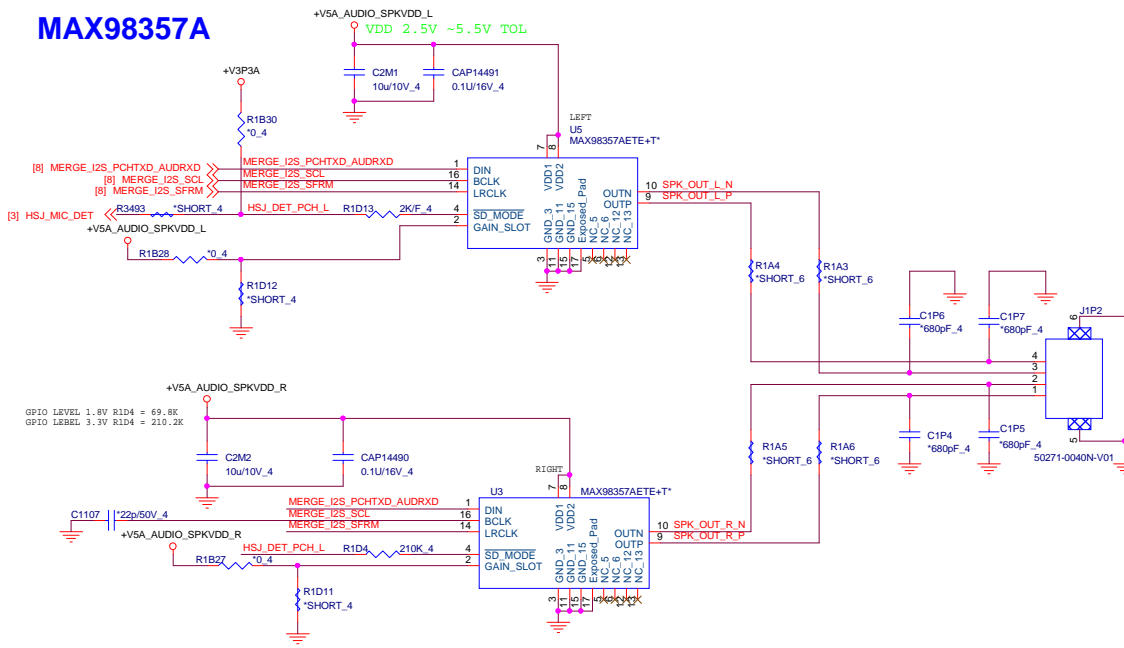
TCH PNL/KB/TRKPAD/FAN



For test only



MAX98357A



LRCLK POLARITY

PART NUMBER	LRCLK POLARITY (LEFT CH)
MAX98357A	LOW
MAX98357B	HIGH

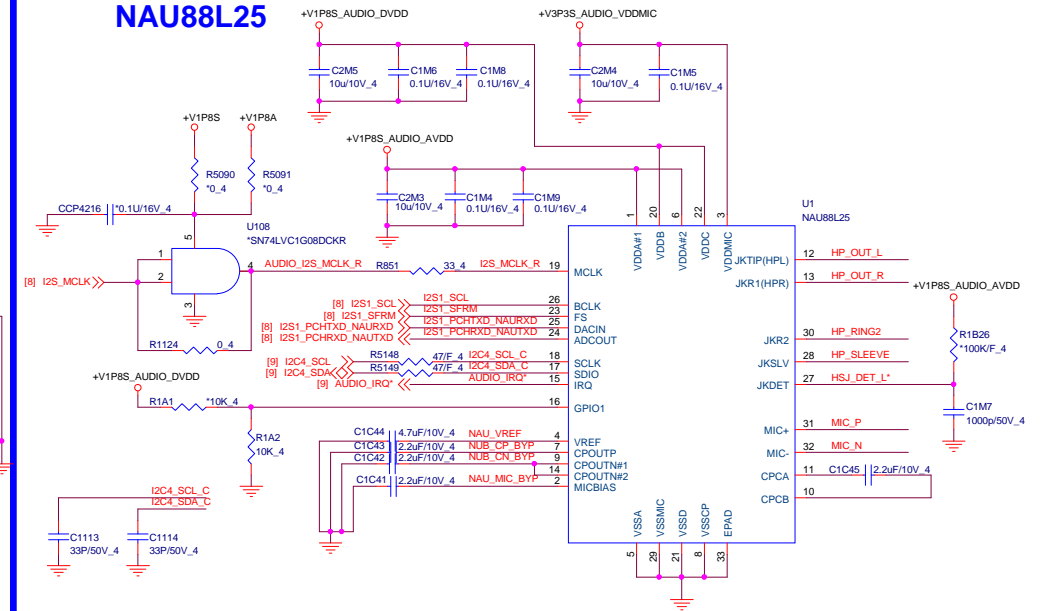
BCLK POLARITY

MODE	PART NUMBER	BCLK POLARITY
I2S	MAX98357A	Rising edge
Left Justified	MAX98357B	Rising edge
TDM	MAX98357A	Rising edge
	MAX98357B	Falling edge

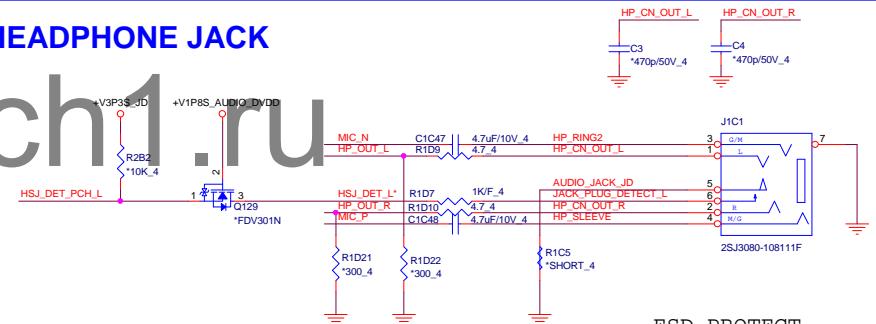
GAIN TABLE

GAIN_SLOT	GAIN(dB)
PL 100K TO GND	15
PL 10K TO GND	12
FLOATING	9
PU TO VDD	6
PU 100K TO VDD	3

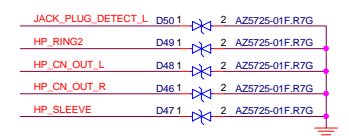
NAU88L25



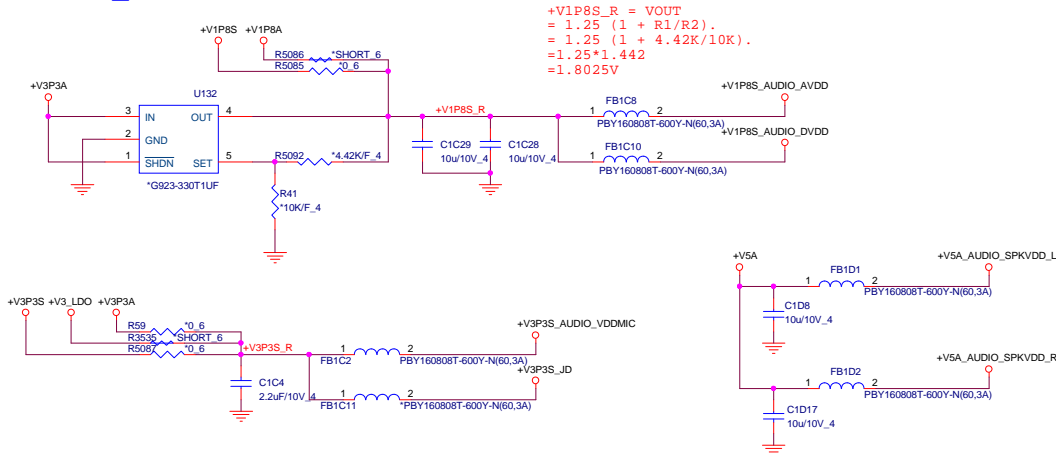
HEADPHONE JACK



ESD PROTECT

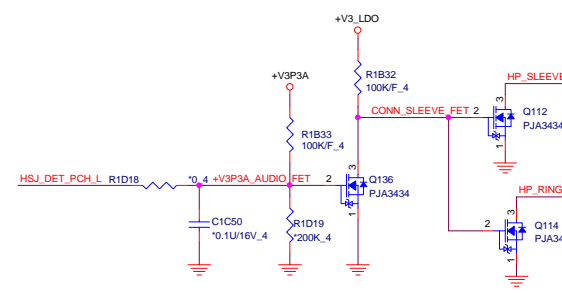


AUDIO_PD




Mic PULL DOWN

Note:
For Rev B Codec,
all components in Mic Pull Down circuit can be DNI.



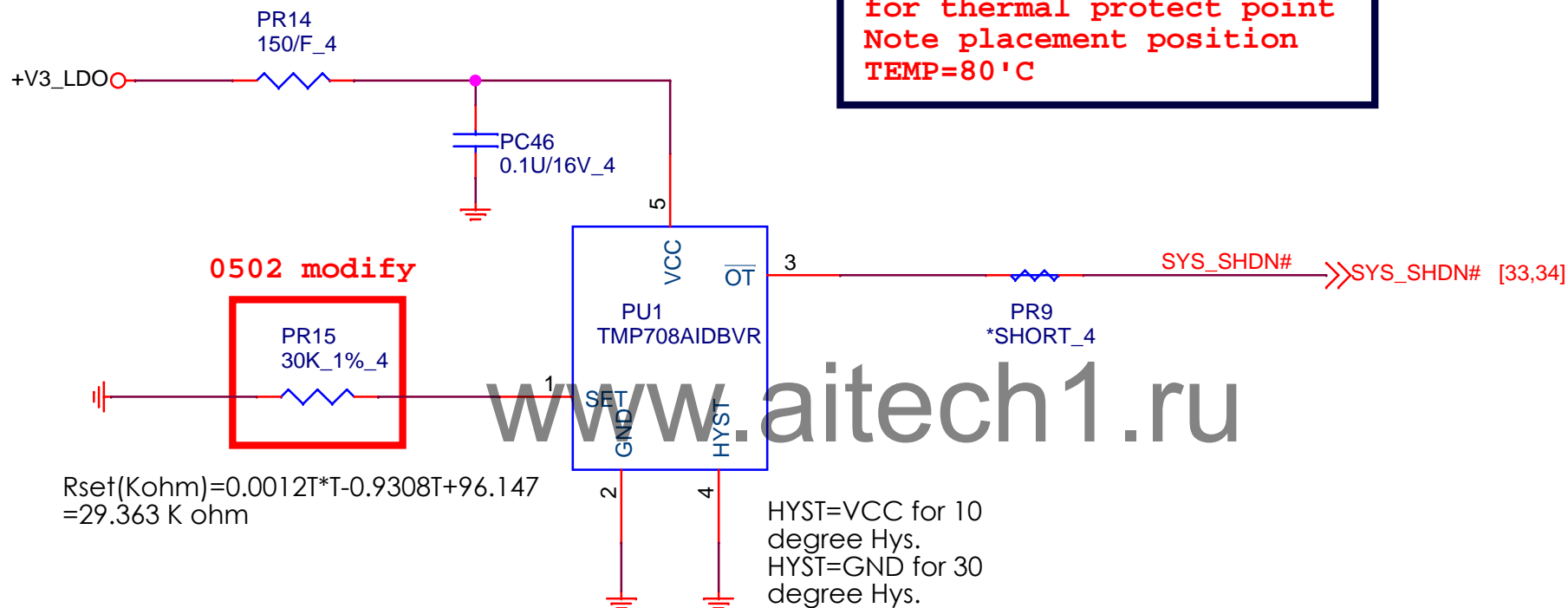
X8: Metal



 Quanta Computer Inc. PROJECT : ZHD		Rev 8A
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	MEC1322	
Date	Yusufur Mar 23, 2017	Phone 20 01 41

Thermal Protection

Need fine tune
for thermal protect point
Note placement position
TEMP=80'C



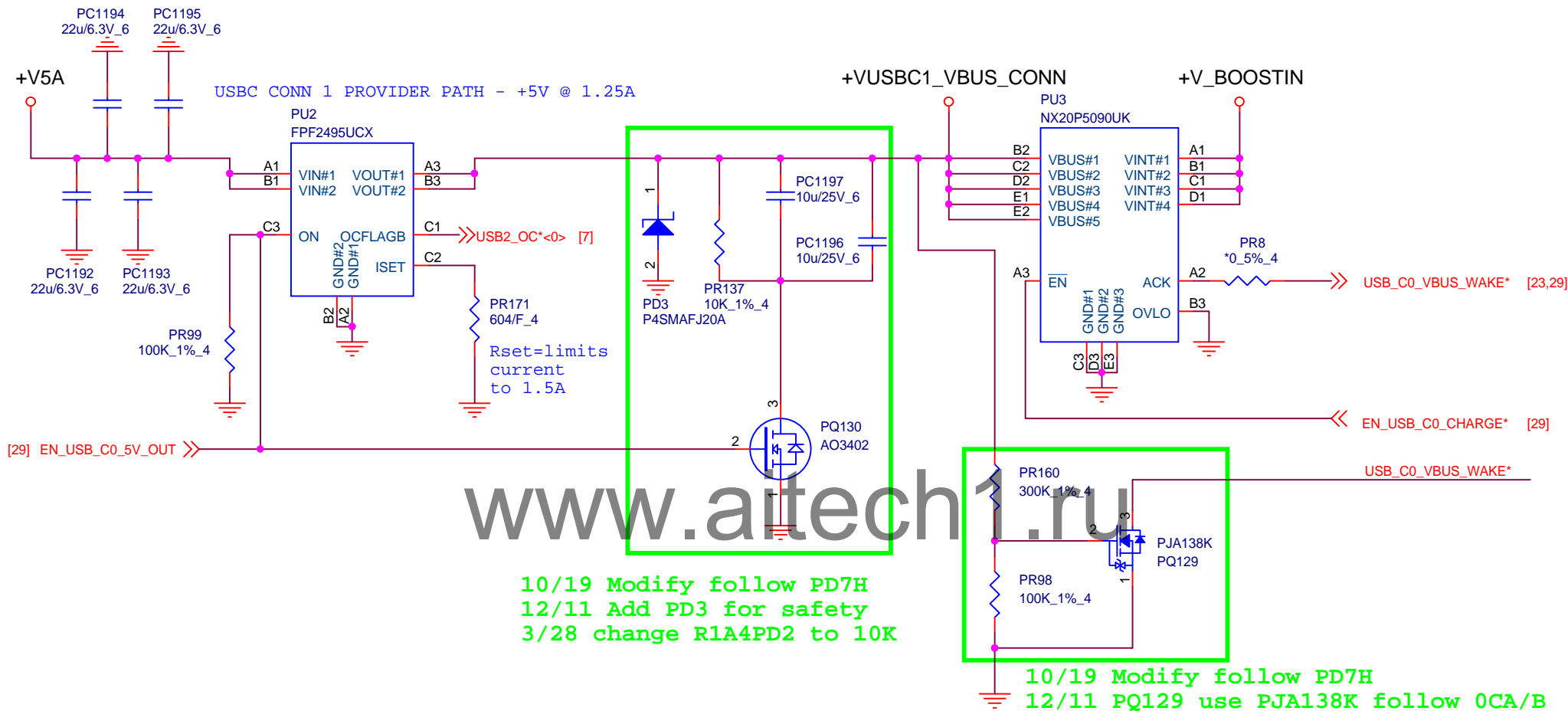
Quanta Computer Inc.

PROJECT : ZHD

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Thermal Protect		

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USBC-PD



Quanta Computer Inc.

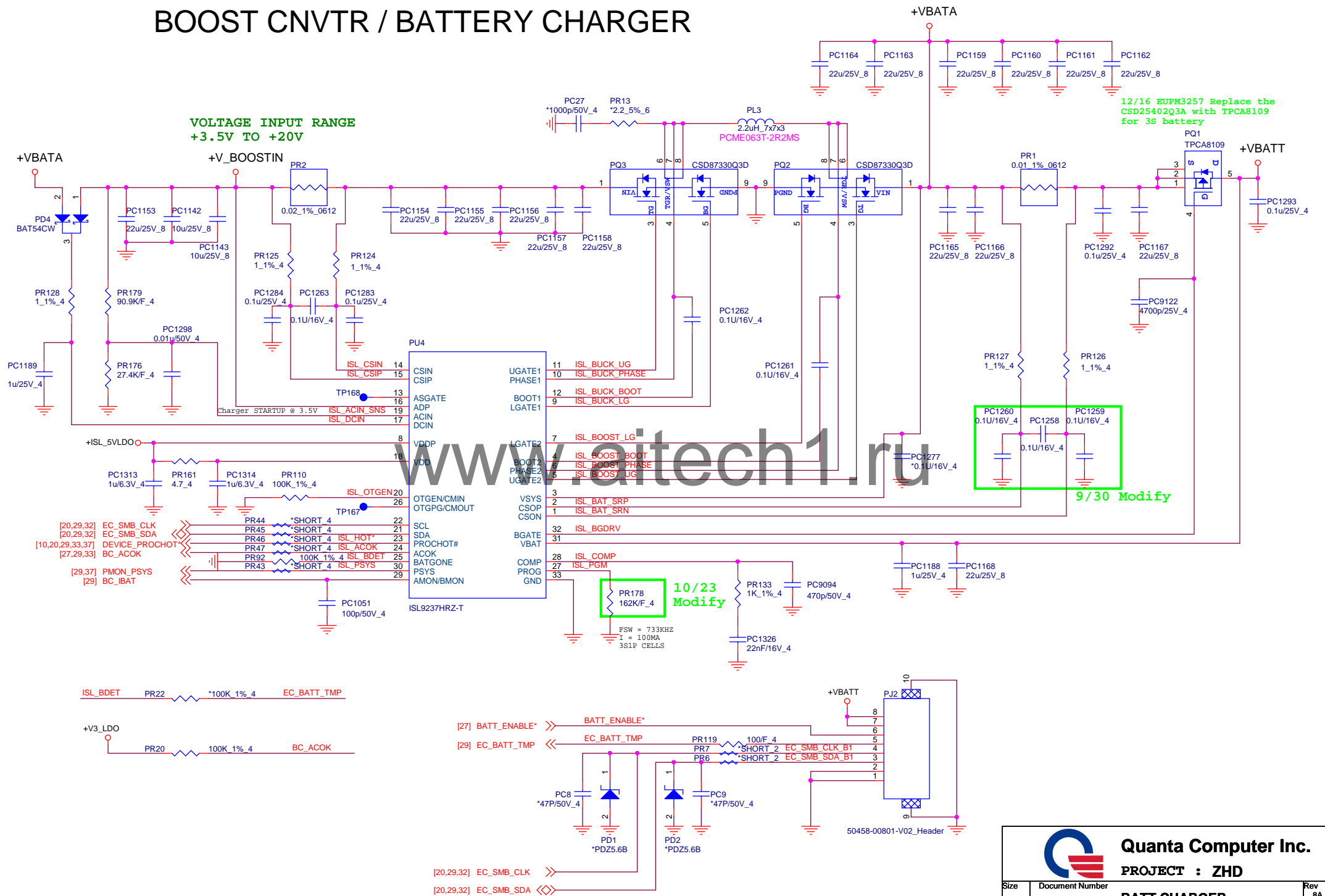
PROJECT : ZHD

Size	Document Number	Rev
	USBCPD	8A

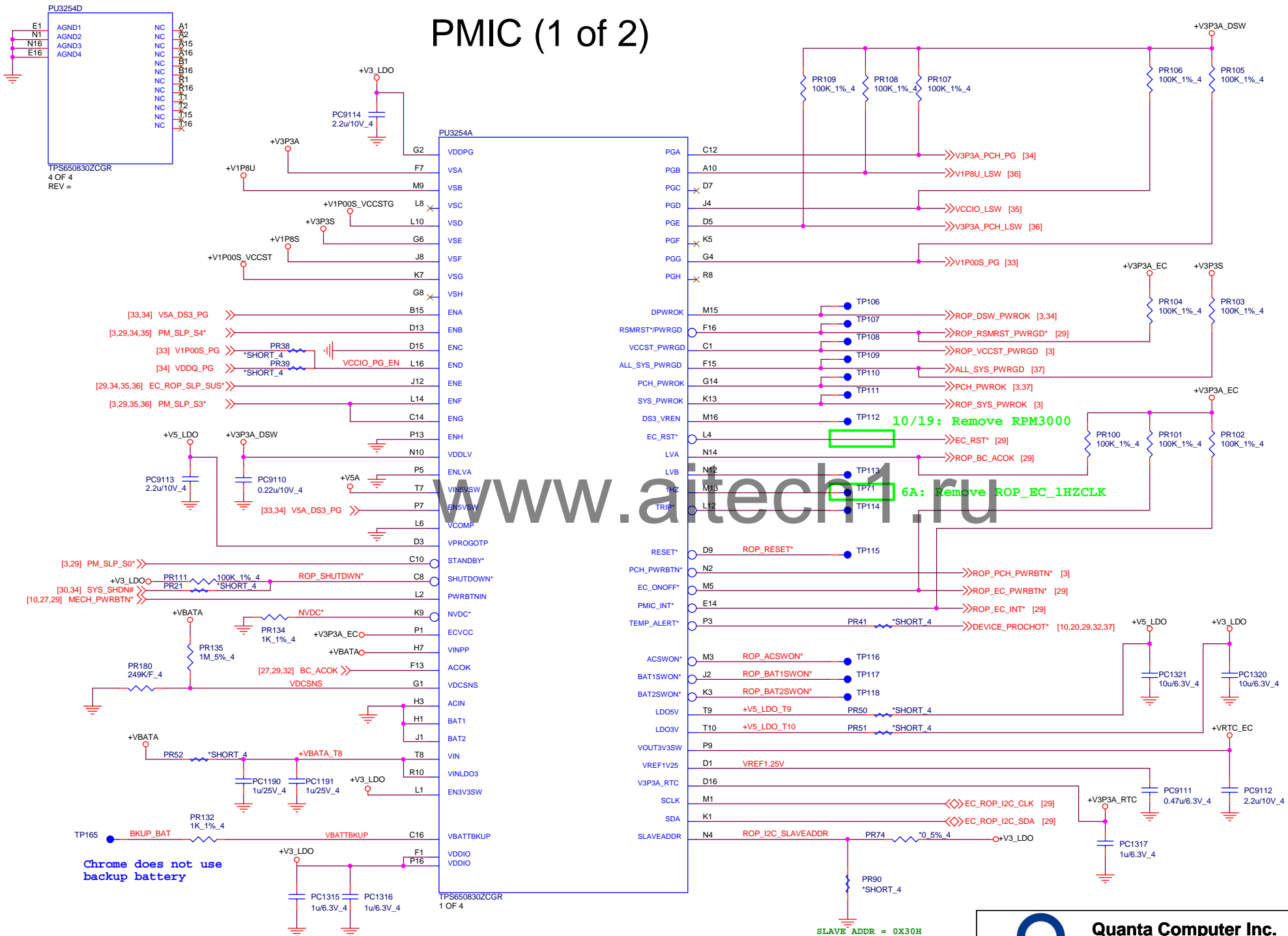
Date: Tuesday, May 23, 2017

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BOOST CNVTR / BATTERY CHARGER



PMIC (1 of 2)



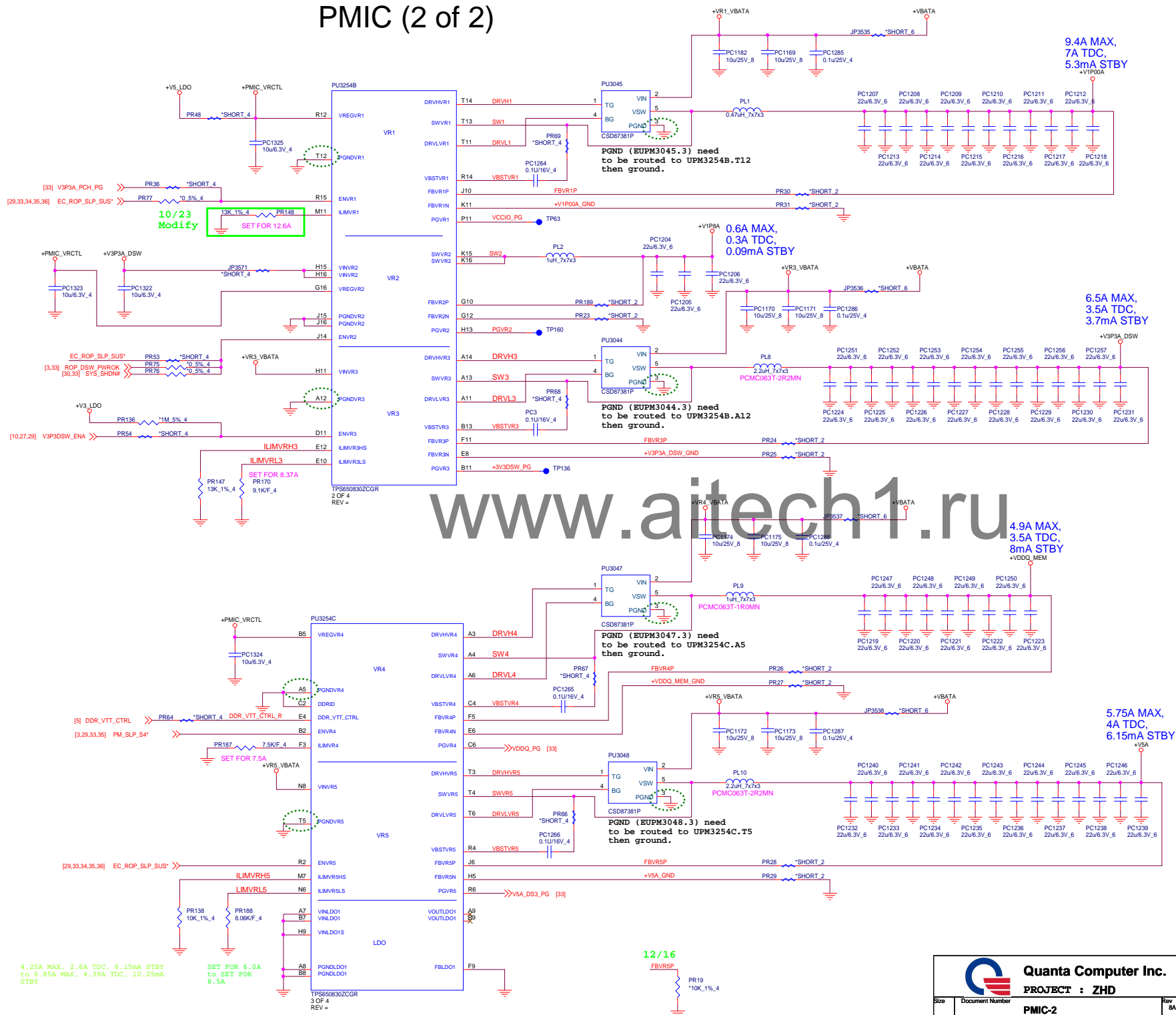
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PROJECT : ZHD

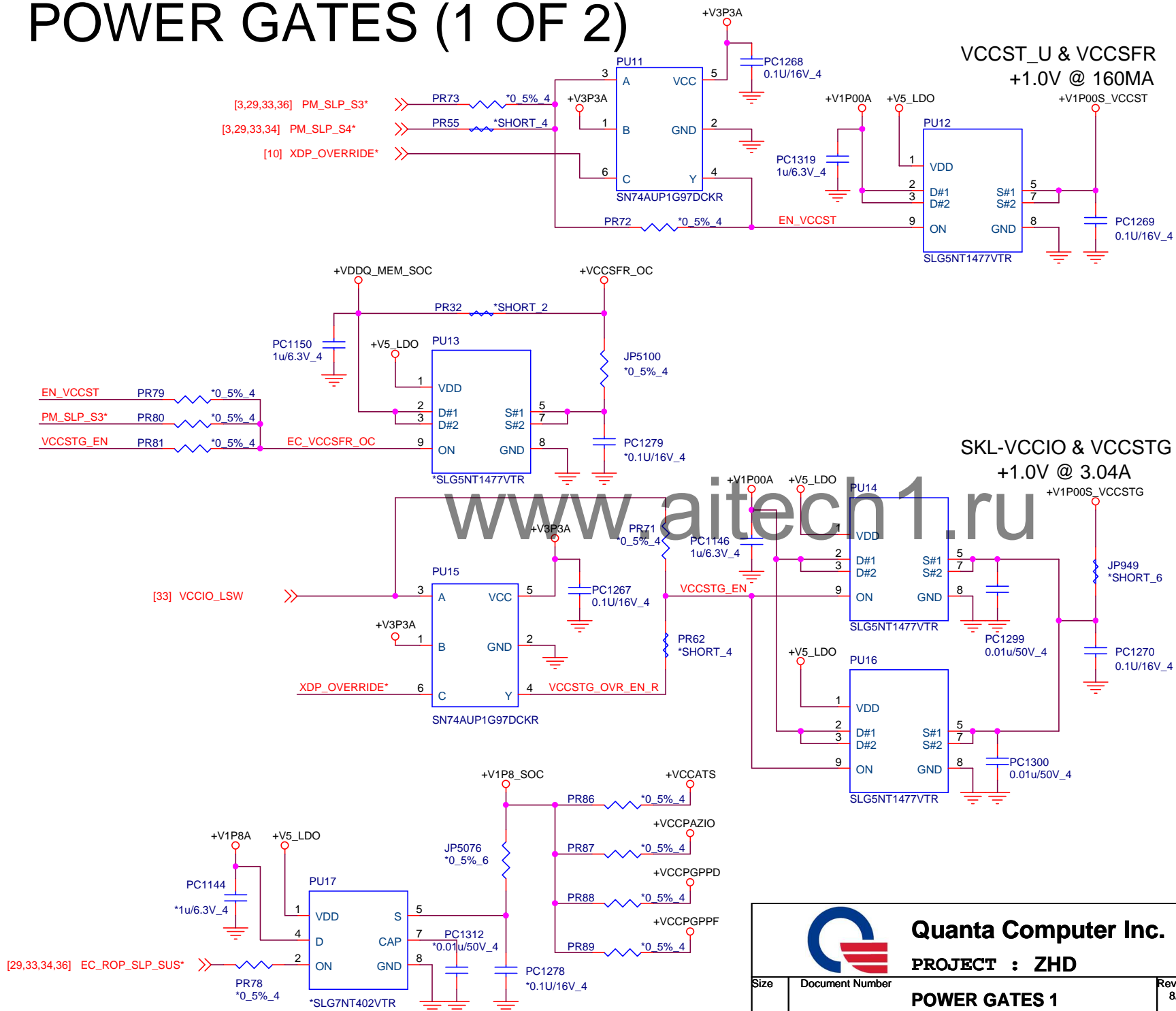
PMIC-1

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PMIC (2 of 2)



POWER GATES (1 OF 2)



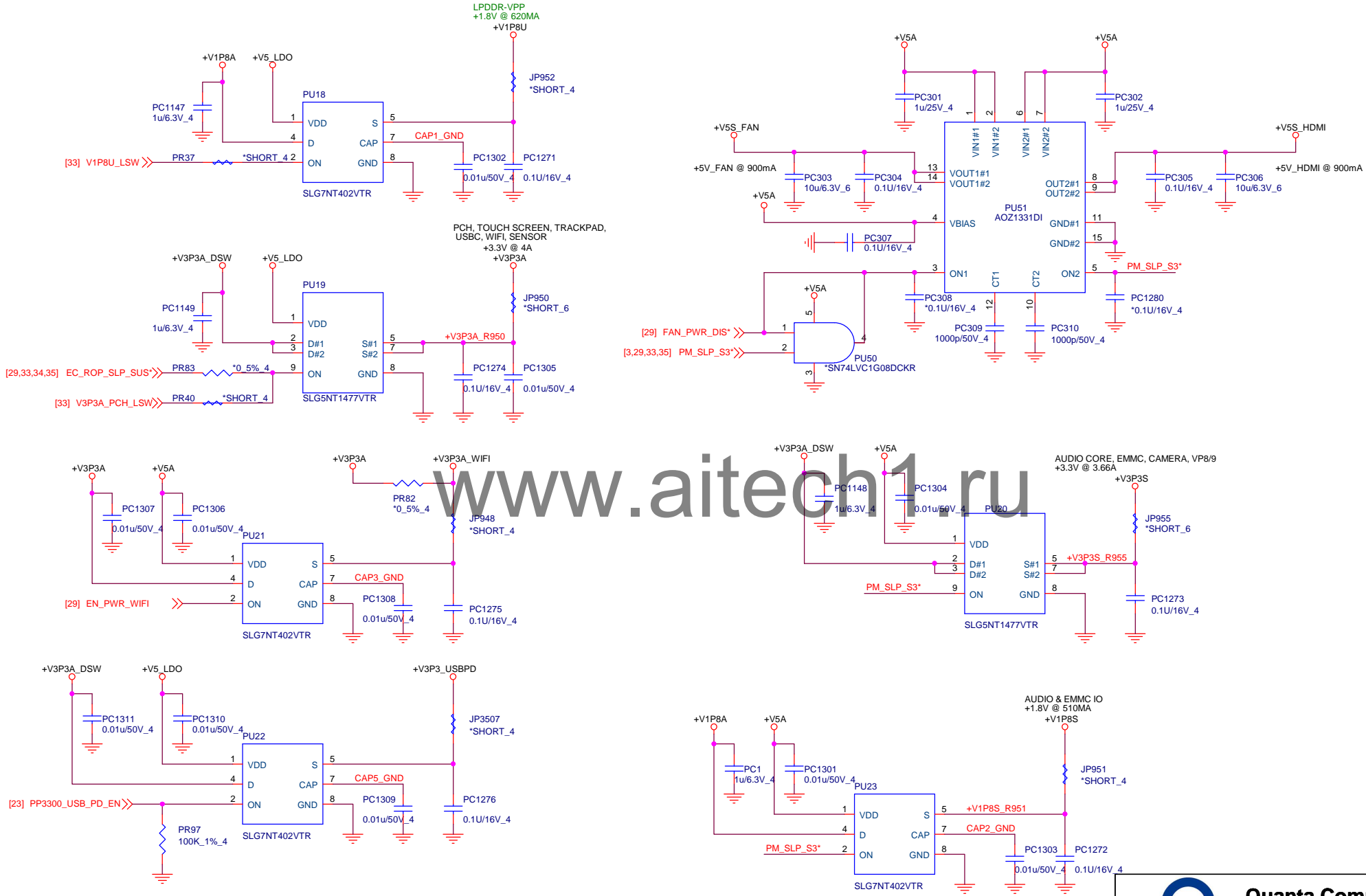
Quanta Computer Inc.

PROJECT : ZHD

POWER GATES 1

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POWER GATES (2 OF 2)

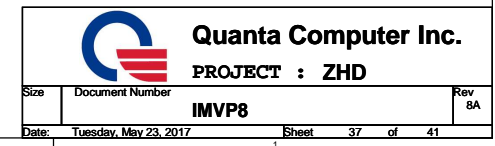


Quanta Computer Inc.
PROJECT : ZHD

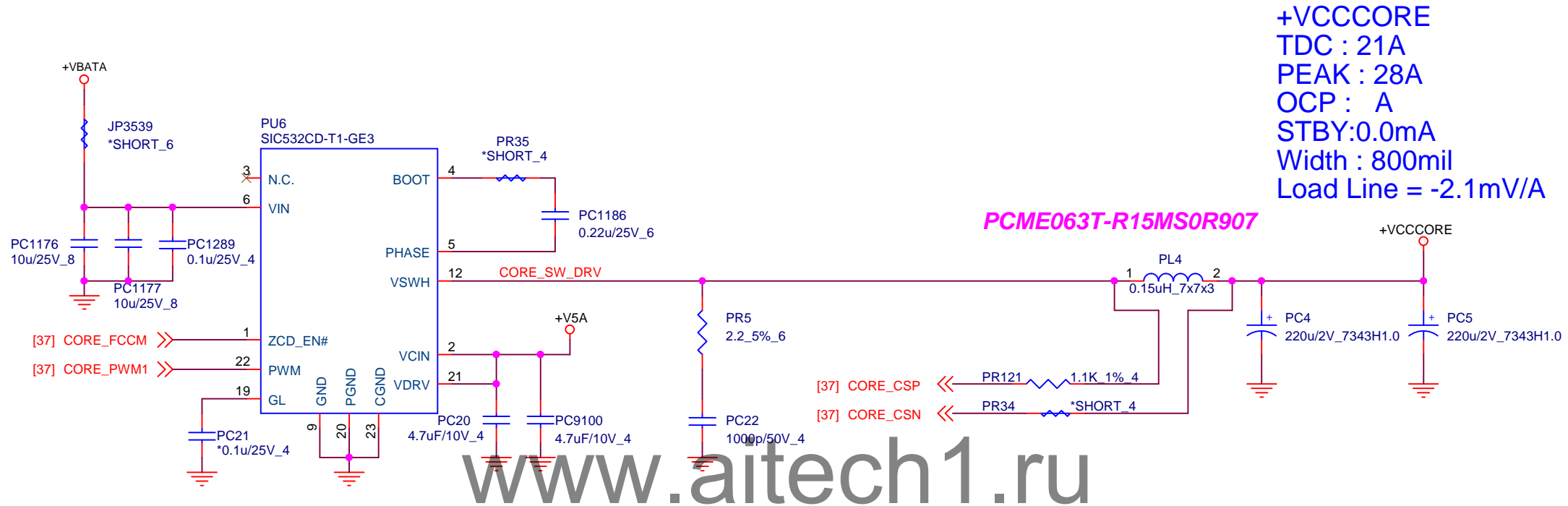
Size	Document Number	Rev
	POWER GATES 2	8A

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(Please tune with VRTT tool and verify the IMVP BOM with Intersil if the PCB layout is changed)



IMVP8 VCCCORE



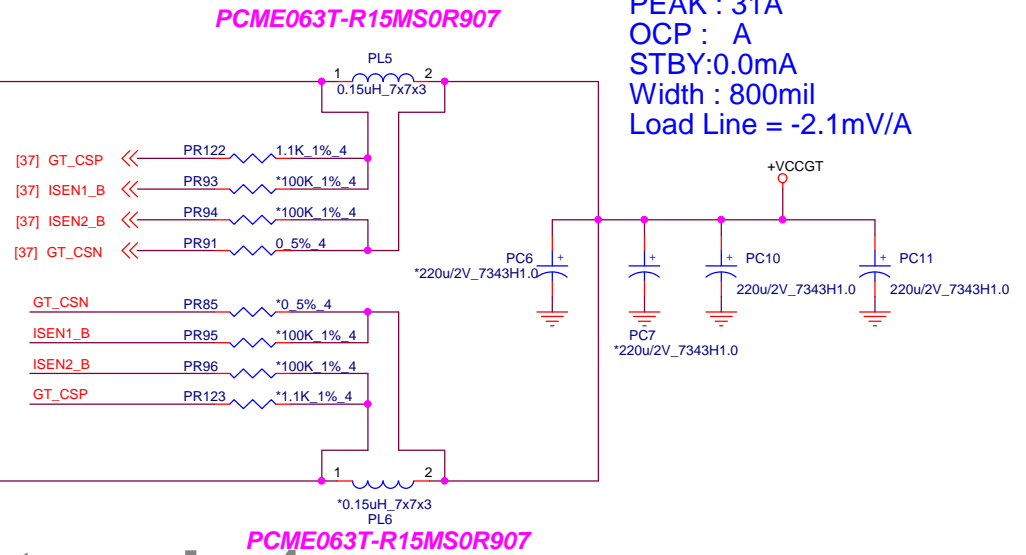
Quanta Computer Inc.

PROJECT : ZHD

IMVP8 CORE

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4.5A MAX,
4A TDC,
0.0mA STBY



